Asynchronous Sigma Delta Modulators for Data Conversion

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Declaration of Originality

I hereby declare that this thesis and the work reported herein was composed by and originated entirely from me. Information derived from the published and unpublished work of others has been acknowledged in the text and references are given in the list of sources.

Copyright Declaration

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Abstract

The research carried out in this thesis focuses on introducing solutions to solve issues existed in asynchronous sigma delta modulators including complex decoding scheme, lacking of noise shaping and effects of limit cycle components. These issues significantly limit the implementation of ASDMs in data conversion.

The first innovation in this work is the introduction of a novel decoding circuit to digitise the output signal of the asynchronous sigma delta modulator. Compared with the conventional decoding schemes, the proposed one does not limit the input dynamic range of ASDMs, and can obtain a high resolution without a fast sample clock. The proposed decoding circuit operates asynchronously and can measure the duty cycle of the modulated square wave without measuring its instantaneous period.

The second innovation of this work is the introduction of a novel architecture of the asynchronous sigma delta modulator with noise shaping without an additional loop filter. Moreover, the proposed modulator requires only a single-bit digital-to-time converter in the feedback loop even for a multi-bit quantiser. The quantiser in the modulator is realized by an eight-phase poly-phase sampler in order to reduce the requirement of the sample clock. Simulation demonstrate that the SNDR of the proposed modulator can be improved by 20dB.

The final innovation of this work is the introduction of frequency compensation to the asynchronous sigma delta modulator. In this proposed modulator, the limit cycle frequency is controlled by the delay time of a novel high linear performance delay line, which is operated in current mode. The compensation is realized by adjusting the equivalent delay time for different input voltage values. The proposed one can double the signal bandwidth with the same limit cycle frequency.

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List of Symbols

A list of the major symbols, notations and abbreviations with their definitions are as follows:

$\lvert\ \rvert$	Absolute value
$\otimes$	Convolution
Re	Real part of a complex number
Im	Imaginary part of a complex number
$FT(\ )$	Fourier transfer function
B	Signal bandwidth
f_0	Output instantaneous frequency
f_c	Limit cycle frequency
T_s	Period of sample clock
T_{ref}	Period of reference clock
μ	Input signal frequency
τ	Delay time of the delay line
T_{DR}	Dynamic range of the delay line
A_0	Open loop gain
$\Delta\tau$	Propagation delay time
e_1 / ε	Quantisation error
L	Order of the loop filter
V	Normalized input signal amplitude
α	Duty cycle of the data signal
F	Carrier-to-bandwidth ratio
NC	Output of the coarse measurement
NF	Output of the fine measurement
b	Hysteresis of the comparator
p	Pole frequency of the loop filter

$k = 1/RC$	Integration gain
Δ_3 /HD_3	The third order distortion
gm	Transconductance
V_{fb}	Amplitude of the feedback signal
I_{bias}	Bias current
I	Current
$V_{control}$	Control voltage of the delay line
C_{ox}	Oxide capacitance of the gate-to-body per unit area
μ_n	Electron mobility in the induced n channel
μ_p	Electron mobility in the induced p channel
Δ	Minimum quantisation step
Δt_0	Delay time of the delay line
SC	Switch capacitor
STF	Signal transfer function
NTF	Noise transfer function
SNR	Signal-to-noise ratio
$SQNR$	Signal-to-quantisation noise ratio
$SFDR$	Spurious-free dynamic range
$SNDR$	Signal-to-noise and distortion ratio
OSR	Oversampling ratio
ADC	Analogue-to-digital converter
DAC	Digital-to-analogue converter
SDM	Sigma delta modulator
PWM	Pulse width modulator
$DT-SDM$	Discrete-time sigma delta modulator
$CT-SDM$	Continuous-time sigma delta modulator
ASDM	Asynchronous sigma delta modulator
NTZ	Non-return-to-zero
RZ	Return-to-zero

HZ	Hold-return-to-zero
VDL	Vernier delay line
VCDL	Voltage controlled delay line
TDC	Time-to-digital converter
TL	Translinear loop
DTC	Tine-to-digital converter
PLL	Phase locked loop
DLL	Delay locked loop
LPF	Low pass filter
TMSP	Time-mode signal processing
INL	Integral non-linearity
DNL	Differential non-linearity
LSB	Least significant bit
OTA	Operational transconductance amplifier
Gm-C	Transconductor-capacitor circuit

Introduction

1.1 Motivation

Despite its long history, the sigma delta modulator remains one of the most popular data converter circuits. Conventionally, sigma delta modulators are widely implemented in low-speed, high-resolution applications. Low power consumption is a particularly important feature in portable applications, leading to long battery life. Consequently, power-efficient architectures such as continuous-time sigma delta modulators have been attracted more attention in recent years.

Continuous-time sigma delta modulators use a cascade of several loop filters to establish a high order noise shaping, so as to realize a high resolution. A single-bit digital-to-time converter (DAC) inherently linear, is implemented in the feedback loop for reasons of circuit simplicity and low power consumption. However, the single-bit quantizer in the forward path will raise stability issues in high order modulators [1]. To solve this issue, a multi-bit internal quantizer is often used to obtain sufficient gain for implementing a stable sigma delta loop filter. This creates another issue: An equivalent high resolution DAC is required in the feedback loop, which increases the complexity of the modulator and the power consumption.

Continuous-time sigma delta modulators require a high sampling frequency to obtain an equivalent over-sampling ratio, in order to improve performance. High sampling frequency not only means increased power dissipation of the clock and sampler, but also increases the design and simulation time and the power consumption of the wideband loop and decimation filters. All this limits sigma delta modulators to ultra-low power applications, such as biomedical and environmental sensors. Other design issues around continuous-time sigma delta modulators include propagation delay and sensitivity to clock jitter. Propagation delay undermines dynamic stability and introduces the need for compensation.

In fact, there does exist another type of sigma delta modulators, named asynchronous sigma delta modulators (ASDM), which has potential properties to solve this issue. ASDMs can be considered as a special type of continuous-time sigma delta modulators. Unfortunately, in current CMOS technology, ASDMs are difficult to implement in data conversion, because of some critical issues. Most significant drawback is the absence of effective circuit to digitise the modulated signal. Other issues which can be resolved including the signal bandwidth which is limited by the limit cycle components and lacking of shaping for quantisation errors. This thesis presents solutions to solve these issues.

1.2 Objectives

This thesis presents studies of the asynchronous sigma delta modulator and proposes solutions to their limitations.

1. Improve a decoding scheme for ASDMs. In the first instance, I noticed that conventional decoding schemes for asynchronous sigma delta modulators limit input dynamic range of modulators, and always requires a high speed sampling clock. This is because conventional decoding schemes can only measure the time interval not the duty cycle of the square wave, and they always use a fast sample to digital the location of the time interval rather than its exact the time value. In order to obtain the duty cycle, two decoding schemes are required to measure both the pulse width and the period, which doubles the chip area and power dissipation. To solve this issue, I introduce a novel decoding scheme for asynchronous sigma delta modulators, which can convert the duty cycle of modulated square wave into digital signals directly. The proposed decoding scheme is realized by a special coarse-fine time-to-digital converter (TDC), and it can measure the duty cycle of the data signal without knowing its instantaneous period.
2. Improve the architecture of ASDMs to introduce noise shaping. I found that the conventional architecture of asynchronous sigma delta modulators with noise shaping with additional loop filter and feedback loop is not efficient. Because the loop filter in the ASDM does not contribute to shape the quantisation errors. And it requires a high resolution digital-to-analogue converter (DAC) in the feedback loop, which increases the design challenge and the complexity of the circuit. Compared with the same system order

synchronous-time sigma delta modulator, the conventional architecture has poorer performance.

3. Improve the architecture of ASDMs to minimize effects of limit cycle components. Finally, I noticed that the limit cycle components of asynchronous sigma delta modulators significantly limit the signal bandwidth of modulators, and it also requires a powerful decimation filter to supply a high attenuation for out-band components. This issue makes ASDM difficult to implement. To overcome this issue, another architecture of ASDMs is implemented, where the limit cycle frequency is determined by the delay time of a delay cell. It give an opportunity to stable the frequency of the output by controlling the delay time of the delay cell. The proposed ASDM works as an ideal pulse width modulator (PWM), which increases design space of decoding circuits, and reduces the requirement of the decimation.

1.3 Outline of this thesis

The thesis is organized in 6 chapters, including the present one. A brief summary of each chapter is given below.

Chapter 2 provides a brief literature review of sigma delta modulators in past five years. A detailed system analysis of asynchronous sigma delta modulators is presented, including fundamental analysis, noise performance and non-idealises.

Chapter 3 presents the implementation of an asynchronous sigma delta modulator with a novel decoding circuit. It discusses the issues of conventional decoding circuits, and introduces a new decoding methodology to overcome these issues. It also presents the architecture of the proposed modulator and decoding circuit in some details, along with simulation results.

Chapter 4 introduces a novel architecture of asynchronous sigma delta modulators with noise shaping. It solves the issues of conventional architectures of asynchronous sigma delta modulators with noise shaping, and presents the details of system analysis and circuits design. The results of the system analysis are illustrated by transistor level simulation results of modulator circuits.

Chapter 5 presents improvements of the asynchronous sigma delta modulator leading to a constant output frequency. This is achieved by the introduction of a compensation block. The methodology of frequency compensation is presented in detail. This chapter concludes with transistor-level simulation results of the entire modulator circuits in an AMS $0.35\mu m$ CMOS process.

Chapter 6 presents some concluding remarks, outlines the limitations of the thesis and discusses some potential directions for future research.

Sigma Delta Modulation Fundamentals

1.4 Introduction

Analogue-to-Digital converters (ADCs) are key building blocks in electronic systems, including as audio, communication, industry measurement and sensor interfaces. Together with digital-to-analogue converters (DACs), they interface analogue real world signals to the digital signal processing system. Application requirements, such as speed, resolution and power consumption, dictate specific ADC architectures to optimise trade-off between power, speed and performance. The sigma delta analogue-to-digital converters are preferred in high-resolution, low-speed applications. Sigma delta converters use oversampling, error processing, and feedback to improve the resolution of the quantiser. In other words many samples of the input signal taken at a high rate are used to produce an output signal at the Nyquist rate. Sigma delta converters are feedback devices operating in closed-loop mode; this makes them tolerant to some analogue imperfections, including offset and mismatch. Additionally, signal processing in a sigma delta analogue-to-digital converter is partitioned between analogue and digital sub-sections; analogue filtering is employed for quantisation error rejection from the signal band, while digital filtering is used to increase the effective resolution by eliminating the out of band quantisation noise [2]. The single-bit sigma delta converter is inherently monotonic and requires no laser trimming [1]. It also lends itself to low cost CMOS foundry processes because of the digitally intensive nature of the architecture. This chapter will present the fundamentals of both synchronous and asynchronous sigma delta modulators.

1.5 Synchronous sigma delta modulators

1.5.1 Discrete-time sigma delta modulator

Discrete-time sigma delta analogue-to-digital converters make use of two basic ideas: oversampling and noise shaping, to decrease the quantisation error power within the signal band and increase the resolution of the conversion. The basic system diagram of a discrete-time sigma delta analogue-to-digital converter is shown in Fig. 2-1. It includes three basic components: an

anti-aliasing filter, a discrete-time sigma delta modulator and a decimator (a digital filter and a down-sampler).

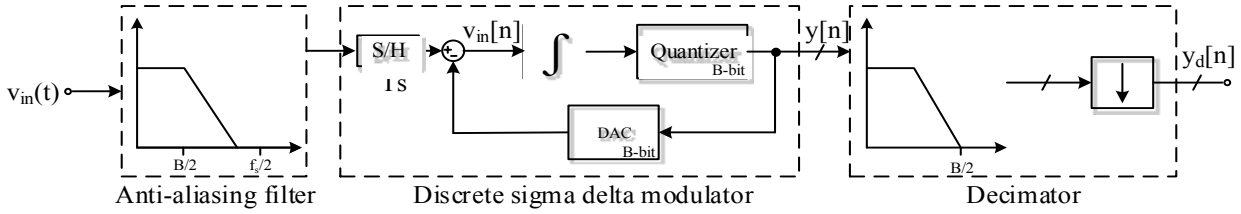


Figure 0-1: Block diagram of a discrete-time sigma delta analogue-to-digital converter

The function of the anti-aliasing filter is to attenuate the out-band components of the input signal so as to avoid aliasing during sampling process. The basic fundamental operations of discrete-time sigma delta modulators is to enclose a simple quantiser in a feedback loop in order to shape the spectrum of both the input signal and the quantisation noise. Typically, the signal is low passed, while the baseband noise is shifted to higher frequencies, and can be suppressed by the filter. This process, known as noise shaping, makes sigma delta modulators much more robust than other analogue-to-digital converters. The output signal of the modulator is fed into a digital filter which attenuates the out-band frequency components and noise. Finally the output signal is down-sampled to the Nyquist rate.

The transfer function of the modulator can be obtained in the z-domain by:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2-1}$$

Where $X(z)$ and $E(z)$ are the z-transform of the input signal and the quantisation error, respectively; $STF(z)$ and $NTF(z)$ are the respective transfer functions for the input signal and quantisation error, which are determined by the architecture implemented by the modulator. According to Fig. 2-1, they are given by

$$\begin{cases} STF(z) = \dfrac{H(z)}{H(z)+1} \\ NTF(z) = \dfrac{1}{H(z)+1} \end{cases} \tag{2-2}$$

Where $H(z)$ is the loop filter transfer function. By implementing a simple ideal loop filter:

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2-3}$$

Eq. (2-1) can be extended to an L^{th} order system yields:

$$Y(z) = z^{-L}X(z) + (1-z^{-L})E(z) \tag{2-4}$$

Ideally, the dynamic range of the L^{th} order sigma delta modulator is:

$$DR \approx 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log_{10}(OSR) \tag{2-5}$$

Where $OSR = f_s/2B$ is the oversampling ratio; N is the bit of the quantiser.

The dynamic range of the modulator will, in general, be limited by quantisation noise and circuit imperfections.

1.5.2 Continuous-time sigma delta modulator

The first recognizable sigma delta modulator, introduced in 1962, was actually implemented as a continuous-time circuit [3]. However, because of the excellent performance of switched-capacitor circuits, most sigma delta modulators are implemented as the discrete-time mode. Switched-capacitor sigma delta modulators are still very popular in middle frequency applications because of their insensitivity to signal waveform. As the time constants of switched-capacitor integrators scale with sampling frequency, switched capacitor modulator circuits allow for greater system flexibility [4].

However, continuous-time sigma delta modulators are attracting attention once again thanks to the increasing demand for lower power circuits. Continuous time modulators have a unique benefit, namely the inherent anti-aliasing filtering offered by the continuous-time loop filter. Continuous-time loop filters are much faster than their discrete-time counterparts, making continuous-time sigma delta modulators popular in high-speed analogue-to-digital converters. The configuration of a basic continuous-time sigma delta modulator is shown in Fig. 2-2.

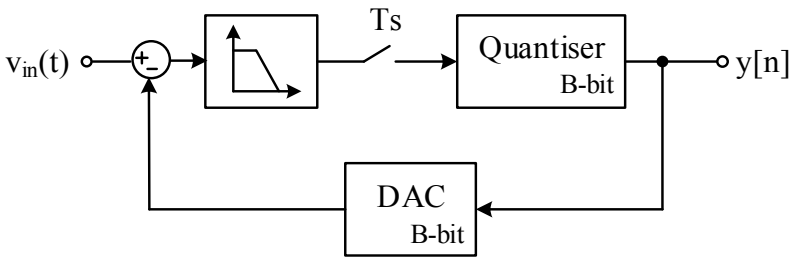


Figure 0-2: Basic configuration of the continuous-time sigma delta modulator with multi-bit quantiser

The architecture of any arbitrary continuous-time sigma delta modulator can be generated by applying a discrete-time to continuous-time transformation to an original discrete-time sigma delta modulator. Depending on the shape of the digital-to-analogue converter impulse response, there are different ways to realizing such a discrete-time to continuous-time transformation. Conventionally, there are three types of conventional digital-to-analogue waveforms: rectangular, triangular and exponential. The rectangular waveforms are easier to implement, while the less popular triangular and exponential waveforms result in better jitter tolerance [5]. Rectangular waveforms include three formats: non-return-to-zero (NRZ), return-to-zero (RZ) and hold-return-to-zero (HZ), as shown in Fig. 2-3. The time definition of these waveforms $R_p(t)$ based on the step function $u(t)$is shown as follows:

$$\begin{cases} R_p(t)\big|_{NRZ} = u(t) - u(t-T) \\ R_p(t)\big|_{RZ} = u(t) - u(t-p) \\ R_p(t)\big|_{HZ} = u(t-p) - u(t-T) \end{cases} \tag{2-6}$$

And the equivalent s-domain forms of eq. (2-7) is:

$$\begin{cases} NRZ(s) = \dfrac{1-e^{-sT}}{s} \\ RZ(s) = \dfrac{1-e^{-sp}}{s} \\ HZ(s) = \dfrac{e^{-sp}-e^{-sT}}{s} \end{cases} \tag{2-7}$$

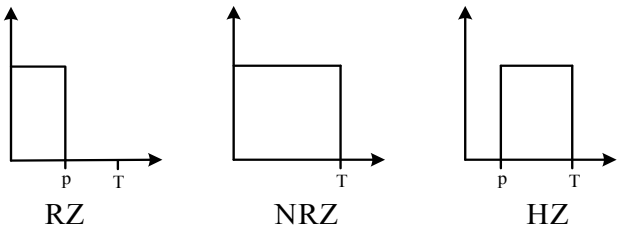


Figure 0-3: Digital-to-analogue converter wave forms for RZ, NRZ, and HZ

Equivalent discrete-time to continuous-time conversions for rectangular digital-to-analogue converter waveforms are listed in Table 2-1.

Table 0-1: Example of z-domain and s-domain sigma delta modulator transformation

Loop filters	1st order low-pass	2nd order low-pass
$H(z)$	$\dfrac{z^{-1}}{1-z^{-1}}$	$\dfrac{z^{-1}\left(2-z^{-1}\right)}{\left(1-z^{-1}\right)^2}$
$H(s)$ (RZ)	$\dfrac{2}{Ts}$	$\dfrac{2+2.5Ts}{(Ts)^2}$
$H(s)$ (NRZ)	$\dfrac{1}{Ts}$	$\dfrac{1+1.5Ts}{(Ts)^2}$

Continuous-time sigma delta modulators have several critical limitations. The first one is related to the excess loop delay. In practice, there exists a certain delay between the quantiser sampling event and the DAC output, caused by the imperfection of circuits implemented in the modulator, such as the finite open loop gain and bandwidth of the loop filter, the propagation delay time in comparator, etc. This delay cause instability of the modulator loop. In intuitive terms, if the DAC feedback waveform is not contained in one sampling period due to the excess loop delay, the effective order of the loop filter is larger than desired; the loop poles move towards the unite circle, and the modulator stability becomes poor. Moreover, the excess loop delay can elevate the quantisation noise floor by degrading the noise transfer function at low-frequencies.

Continuous time sigma delta modulators are also more sensitive to the clock jitter than discrete-time sigma delta modulators; the internal clock not only controls the comparison instant, but also controls the rising and falling edges of the digital-to-analogue converter output. As a result, clock jitter errors are directly added to the input signal. The effect of clock jitter in continuous-time sigma delta modulators has been extensively analysed in the literatures [6-8]. K. Reddy and S. Pavan's work showed that the jitter induced noise in modulators with NRZ feedback is predominantly determined by the out-band behaviour of the NTF, thus more aggressive noise shaping exacerbates the jitter sensitivity.

Many authors have presented solutions to these issues. However, they all focus on the detailed circuit design and some compensation techniques [9-12], which increase the challenge of design, complex of the circuits, and the power dissipation as well. The comparison between DT-SDM and CT-SDM is shown in Table 2-2.

Table 0-2: Comparison between DT-SDM and CT-SDM

	DT-SDM	CT-SDM
Common	• Synchronous modulator • Noise shaping and over-sampling • High order system (at least 2nd order system)	
Advantages	• High resolution • Developed technology	• Inherent anti-aliasing filter • High conversion speed
Disadvantages	• Require pre anti-aliasing filter • Low conversion speed	• Sensitive to clock jitter • Excess loop delay (instability)

	• Instability (high order system)	

1.6 State of the art for the synchronous sigma delta modulator

With the exception of a few milestone works, referenced for completeness, a literature survey on recently published synchronous sigma delta modulators is summarized in Table 2-2. Discrete-time sigma delta modulators are implemented by switched-capacitor or switched-current techniques; continuous-time sigma delta modulators are often realized by active-RC or Gm-C techniques. The signal bandwidth, signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SNDR), and power consumption are key performance metrics that can be used for comparing different designs. Low pass sigma delta modulators are evaluated by two figures-of-merits, namely:

$$FOM_W = \frac{P}{2B \times 2^{ENOB}} \tag{2-8}$$

$$FOM_S = SNDR + 10\log\left(\frac{B}{p}\right) \tag{2-9}$$

FOM_W emphasizes power consumption, whereas FOM_S emphasizes resolution. Better performance of sigma delta modulators is indicated by smaller FOM_w and larger FOM_S values.

The data in Table 2-3 clearly shows that current trend is towards continuous-time sigma delta modulators; an increasing number of published sigma delta modulators are based on the continuous-time approach. In order to form an idea of current design trends, and to compare the potentials of discrete-time and continuous-time implementation, a survey of design approaches is presented here. The survey covers publications in the IEEE International Solid State Circuits Conference (ISSCC) and the IEEE VLSI Conference from 2008 to 2013. Fig. 2-4 shows the Signal-to-Noise-and Distortion (SNDR) versus signal bandwidth of discrete-time and continuous-time implementations. Continuous-time circuits mostly cover the high frequency applications. The higher dynamic range is mostly occupied by low signal bandwidth, discrete-time implementations. A survey of power consumption versus Nyquist output frequency is presented in Fig. 2-5. Note that the continuous-time implementations, even in high frequency applications, still show a lower

power consumption than their discrete-time counterparts. A final comparison is shown in Fig. 2-6 where we can observe that continuous-time converters have better FOM_S than their discrete-time counterparts.

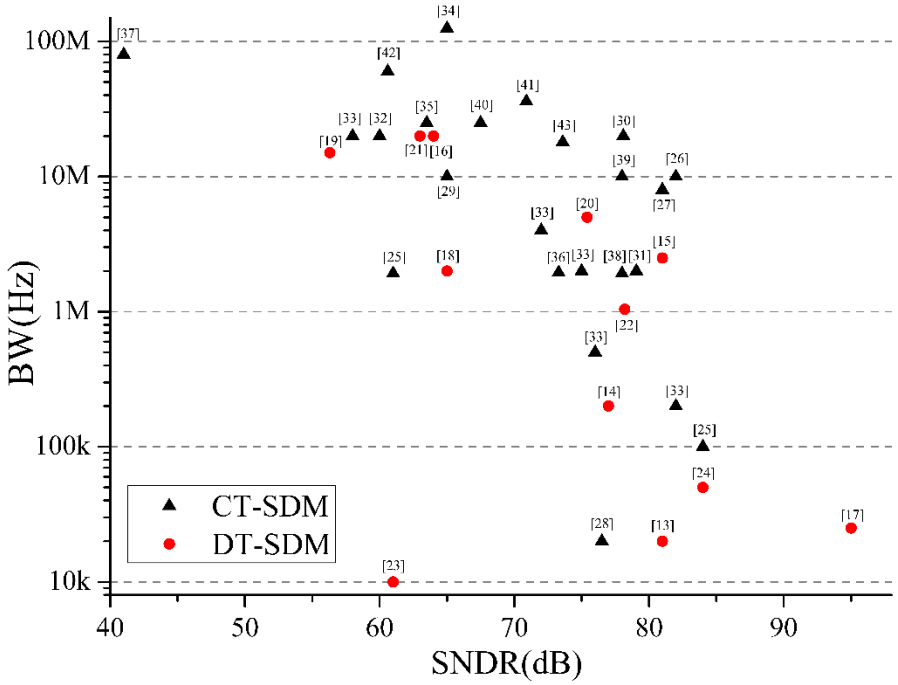


Figure 0-4: SNDR and signal bandwidth of recently published synchronous sigma delta modulators

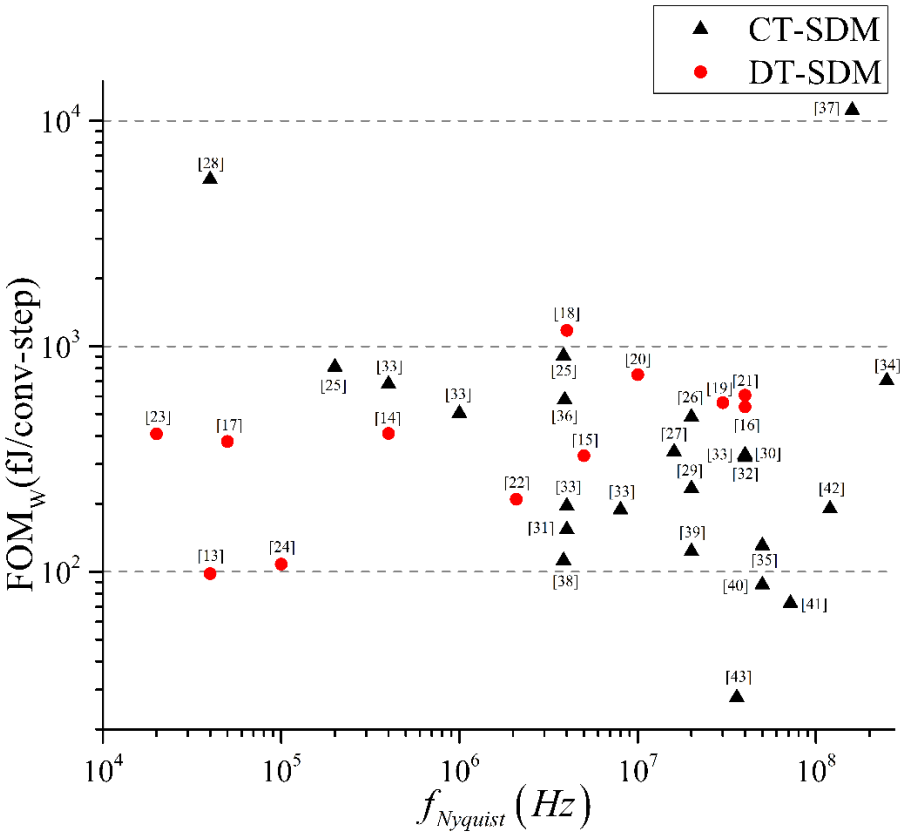


Figure 0-5: FOM_W versus Nyquist output frequency

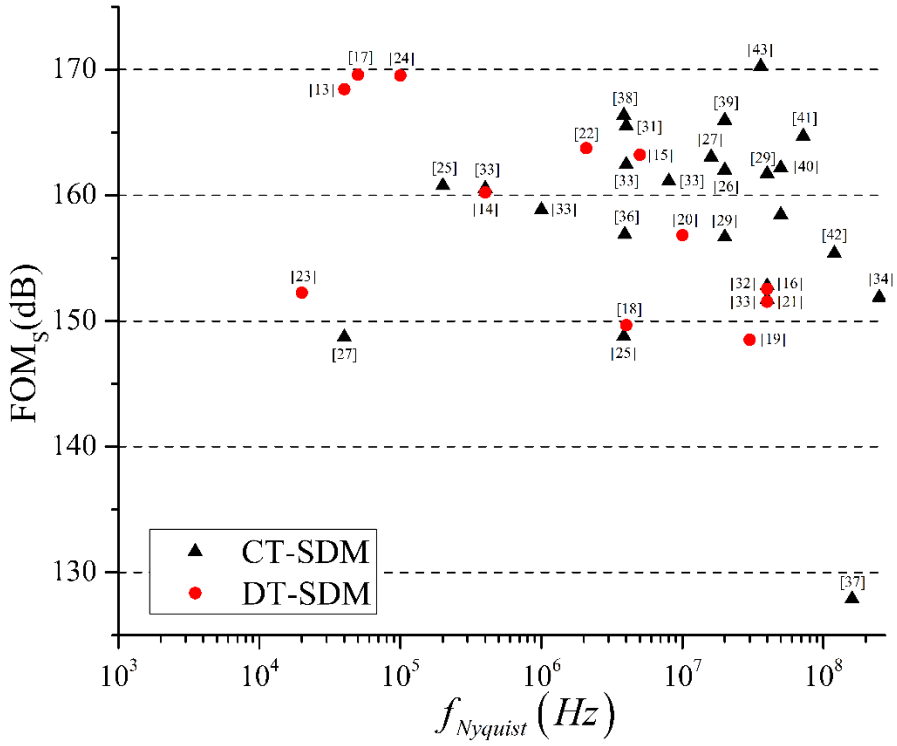


Figure 0-6: FOM_S versus Nyquist output frequency

Table 0-3: State of the art of synchronous sigma delta modulators

Discrete-time sigma delta modulators								
Year	Technology (um)	BW (Hz)	Fs (Hz)	OSR	SNDR (dB)	Power (mW)	FOM_W (fJ/conv-step)	FOM_S (dB)
2008[13]	0.18	2.00E+4	4.00E+6	100	81.0	3.60E-2	98.1	168.4
2008[14]	0.065	2.00E+5	1.50E+8	375	77.0	9.50E-1	410.5	160.2
2008[15]	0.18	2.50E+6	6.00E+7	12	83.0	15.0	327.1	163.2
2008[16]	0.09	2.00E+7	4.20E+8	11	72.0	27.9	538.6	152.6
2008[17]	0.18	2.50E+4	5.00E+6	100	100.0	8.70E-1	378.5	169.6
2009[18]	0.09	2.00E+6	3.20E+8	80	65	6.83	1175.0	149.7
2009[19]	0.045	1.50E+7	1.50E+9	50	56.3	9.00	562.1	148.5
2009[20]	0.18	5.00E+6	8.00E+7	8	75.4	36.0	748.1	156.8
2011[21]	0.032	2.00E+7	4.00E+8	10	63.0	28.0	606.4	151.5
2011[22]	0.18	1.04E+6	5.00E+7	24	78.2	2.90	209.5	163.8
2011[23]	0.13	1.00E+4	1.40E+6	70	61.0	7.50E-3	409.0	152.2
2011[24]	0.18	5.00E+4	1.60E+6	16	84.0	1.40E-1	108.1	169.5
Continuous-time sigma delta modulators								
Year	Technology (um)	BW (Hz)	Fs (Hz)	OSR	SNDR (dB)	Power (mW)	FOM_W (fJ/conv-step)	FOM_S (dB)
2008[25]	0.065	1.00E+5	2.60E+7	130	84.0	2.10	810.5	160.8
2008[25]	0.065	1.92E+6	6.24E+7	16	61.0	3.20	908.9	148.8
2008[26]	0.18	1.00E+7	6.40E+8	32	82.0	100	485.9	162.0
2008[27]	0.065	8.00E+6	2.56E+8	16	81.0	50.0	340.8	163.0
2008[28]	0.045	2.00E+4	1.20E+7	300	76.5	1.20	5492.2	148.7
2009[29]	0.09	1.00E+7	6.40E+8	32	65.0	6.80	234.0	156.7
2009[30]	0.13	2.00E+7	9.00E+8	23	78.1	87.0	331.2	161.7
2009[31]	0.065	2.00E+6	1.28E+8	32	79.1	4.52	153.9	165.5
2009[32]	0.065	2.00E+7	2.50E+8	6	60.0	10.5	321.2	152.8
2010[33] GSM mode	0.09	2.00E+5	5.12E+7	128	82.0	2.80	680.3	160.5
2010[33] BT mode	0.09	5.00E+5	9.60E+7	96	78	2.60	504.2	158.8
2010[33] UMTS mode	0.09	2.00E+6	1.28E+8	32	75	3.60	195.8	162.4

2010[33] DVB-H mode	0.09	4.00E+6	1.92E+8	24	72	4.90	188.3	161.1
2010[33] WLAN mode	0.09	2.00E+7	6.40E+8	16	58	8.50	327.4	151.7
2011[34]	0.045	1.25E+8	4.00E+9	16	65.0	256	704.7	151.9
2011[35]	0.09	2.50E+7	5.00E+8	10	63.5	8.00	130.9	158.4
2011[36]	0.065	1.95E+6	1.25E+8	32	73.3	8.55	580.2	156.9
2011[37]	0.04	8.00E+7	8.88E+9	56	41.0	164	11148.1	127.9
2011[38]	0.04	1.92E+6	2.46E+8	64	78.0	2.80	112.3	166.4
2012[39]	0.09	1.00E+7	6.00E+8	30	78.0	16.0	123.2	166.0
2012[40]	0.09	2.50E+7	5.00E+8	10	67.5	8.50	87.7	162.2
2012[41]	0.09	3.60E+7	3.60E+9	50	70.9	15.0	72.7	164.7
2012[42]	0.045	6.00E+7	6.00E+9	50	60.6	20.0	190.4	155.4
2013[43]	0.028	1.80E+7	6.40E+8	18	73.6	3.90	27.7	170.2

1.7 Asynchronous sigma delta modulators

A new type of sigma delta modulators, originally introduced by Kikkert [44], has recently attracted attention. This type of modulator was forgotten for many years until interest revived due to its perceived potential for high frequency and low power application in the absence of a fast system clock. The dynamics of asynchronous sigma delta modulators were studied in detail by Roza and Ouzounov [45-51]. The comparison between ASDM and CT-SDM is shown in Table 2-4. Both of them have inherent anti-aliasing filters. However, the ASDM has some special properties, including simple circuit design and immunity to clock jitter.

Table 0-4: Comparison between ASDM and CT-SDM

	ASDM	CT-SDM
Common	• Inherent anti-aliasing filter • Low power or high speed applications	
Advantages	• Simple circuit (first order) • Immunity to clock jitter	• Noise shaping
Disadvantages	• Complex decoding scheme • Lack of noise shaping • Limit cycle components	• Complex system (high order) • Sensitive to clock jitter • Excess loop delay (instability)

1.7.1System analysis

An asynchronous sigma delta modulator (Fig. 2-7(a)) includes two functional blocks: an integrator and a hysteretic comparator. The output (Fig. 2-7(b)) is a pulse width modulated square wave of period T with a pulse-width T_1. The duty cycle α is proportional to the amplitude of the input signal (eq. (2-10)). Moreover, the period T of the asynchronous modulator output signal is modulated by the normalized input voltage (eq. (2-11)).

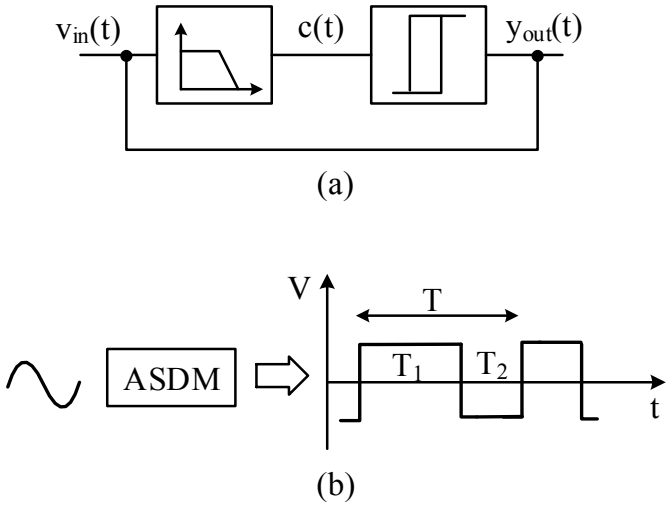


Figure 0-7: (a) System diagram and (b) Timing diagram of the ASDM

$$\alpha = \frac{V+1}{2} = \frac{T_1}{T_1+T_2} \tag{2-10}$$

$$\frac{f_0}{f_c} = \frac{T_1}{T_1+T_2} = 1-V^2 \tag{2-11}$$

In these expressions f_0 is the output carrier frequency and f_c is the maximum value of f_0, namely the limit cycle frequency; $|V|<1$ is the normalized input amplitude.

1.7.1.1 Analysis for DC input signal

Waveforms of asynchronous sigma delta modulators for a constant input signal V ($|V|<1$) are shown in Fig. 2-8. The output of the modulator is a two level signal of constant duty cycle.

Assuming the integration gain of the loop filter $RC = 1$, the positive and negative time intervals can be derived as:

$$T_1[n] = \frac{1}{1+V} \cdot \frac{1}{2f_c} \tag{2-12}$$

$$T_2[n] = \frac{1}{1-V} \cdot \frac{1}{2f_c} \tag{2-13}$$

Where b is the hysteresis of the comparator; $f_c = 1/4b$ is the limit cycle frequency.

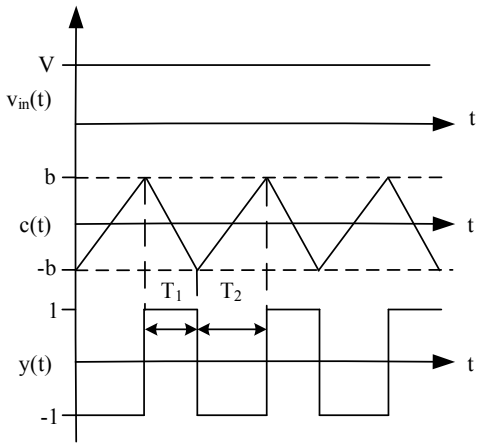


Figure 0-8: Timing diagram of the asynchronous sigma delta modulator with a constant input

The square wave with duty cycle α be represented as:

$$y(t) = 2\alpha - 1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin \alpha n\pi}{n}\cos n\omega_0 t \tag{2-14}$$

From the block diagram in Fig. 2-8 (a), it can be inferred that:

$$\left[v_{in} - y(t)\right] \otimes f(t) = c(t) \tag{2-15}$$

Where $f(t)$ is the pulse response of the loop filter; $c(t)$ is the output of the loop filter; and $\otimes$ denotes a convolution.

According to Appendix I, $c(t)$ can be derived as:

$$c(t)=\left[V-(2\alpha-1)\right]F(0)-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\cdot\left[\mathrm{Re}\,F(n\omega_0)\cos n\omega_0 t-\mathrm{Im}\,F(n\omega_0)\sin n\omega_0 t\right] \quad (2\text{-}16)$$

Based on the boundary conditions:

$$\begin{cases} y(t_1)=1, c(t_1)=b, t_1=-\dfrac{T_1}{2}+k(T_1+T_2) \\ y(t_2)=-1, c(t_2)=-b, t_2=\dfrac{T_1}{2}+k(T_1+T_2) \end{cases} \quad (2\text{-}17)$$

Addition and subtraction of eq. (2-16) based on conditions results in:

$$\begin{cases} \left[V-(2\alpha-1)\right]F(0)=\dfrac{4}{\pi}\displaystyle\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\mathrm{Re}\,F(n\omega_0)\cos n\omega_0\frac{T_1}{2} \\ \displaystyle\sum_{n=1}^{\infty}\frac{\sin^2 n\omega_0\dfrac{T_1}{2}}{n}\mathrm{Im}\,F(n\omega_0)=-\dfrac{\pi b}{4} \end{cases} \quad (2\text{-}18)$$

Assuming the loop filter is an ideal integrator with a transfer function of:

$$F(\omega)=-\frac{1}{j\omega} \quad (2\text{-}19)$$

After a little algebraic manipulation we get the expressions for the frequency and duty cycle of the output signal:

$$\begin{cases} \alpha=\dfrac{1+V}{2} \\ f_0=f_c\cdot(1-V^2) \end{cases} \quad (2\text{-}20)$$

When a zero input is applied, the output of the asynchronous sigma delta modulator is a square wave with duty cycle of 50%. The frequency of the output then reaches its maximum value named as the limit cycle frequency.

1.7.1.2 Analysis for a sinusoidal input signal

With a non-trivial input the system becomes complex to analyse. However, if we assume the input signal is slow changing, in other words, the output instantaneous frequency of the modulator is much higher than that the input signal, $f_c / f_{in} >> 1$, the expression of eq. (2-16) is still valid in one period, $T_m \le t \le T_{m+1}$.

We assume that the input is $v_{in} = V \cos \mu t$, with $|V| < 1$, normalized to the power supply. Here we rewrite the input signal as $v_{in}(T_m) = \sum_{m=1}^{\infty} V \cos \mu T_m$. In one period $T_m \le t \le T_{m+1}$, the input signal can be considered to be constant. When $T_m - T_{m+1} \to 0$, it becomes the original sine wave. In this case, eq. (2-14) can be rewritten as:

$$y(t) = \sum_{m=1}^{\infty} V \cos \mu T_m + \frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\sin n\pi \left(\frac{1 + V \cos \mu T_m}{2} \right)}{n} \cos n\omega_c \int \left(1 - \frac{V^2 + V^2 \cos 2\mu T_m}{2} \right) dt \quad (2\text{-}21)$$

By inserting the boundary conditions eq. (2-15), and based on eq. (I-11) in Appendix I the following equations can be derived:

$$\begin{cases} \left[V \cos \mu T_m - (2\alpha - 1) \right] \mathrm{Re}\, F(\mu) = \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin 2\alpha n\pi}{n} \mathrm{Re}\, F(n\omega_0) \\ \sum_{n=1}^{\infty} \frac{\sin^2 \alpha n\pi}{n} \mathrm{Im}\, F(n\omega_0) = -\frac{\pi b}{4} \end{cases} \quad (2\text{-}22)$$

We are particularly interested in the first harmonic band (n=1) of $y(t)$:

$$y_1(t) = \sum_{m=1}^{\infty} \frac{4}{\pi} \cos \frac{\pi V \cos \mu T_m}{2} \cos \left[\omega_c \left(1 - \frac{V^2}{2} \right) t - \frac{\omega_c V^2}{4\mu_s} \sin 2\mu T_m \right] \quad (2\text{-}23)$$

Here we implement the Jacobi-Anger expansion (Appendix I) to rewrite eq. (2-23) as:

$$y_1(t) = \mathrm{Re}\frac{4}{\pi}\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} J_n\left(\frac{\pi}{2}V\right) J_{2m}\left(\frac{\omega_0 V^2}{4\mu}\right) e^{in(\pi/2-\mu t)} e^{i2m\mu t} e^{im(\pi/2-\omega t)} \tag{2-24}$$

It is clear from eq. (2-24), that the amplitudes and frequencies of the Bessel components are a function of both the amplitude and frequency of the input signal and the limit cycle frequency as well. The high-frequency components are tones at frequencies $f_0 \pm k(2f_{in})$, where k is an integer number. This holds for small-signal amplitudes, $f_0 \approx f_c$ as shown in Fig.2-9.

On the other hand, when V is close to the full scale, the output frequency will decrease. The high frequency components are shifting to the low frequency region, and the tails at adjacent harmonics of f_0 are mixed, as shown in Fig.2-10 Therefore, in practical design, the limit cycle frequency should be set far away from the baseband to avoid these components shifting into signal baseband, and a high order filter is required to attenuate these out-band components.

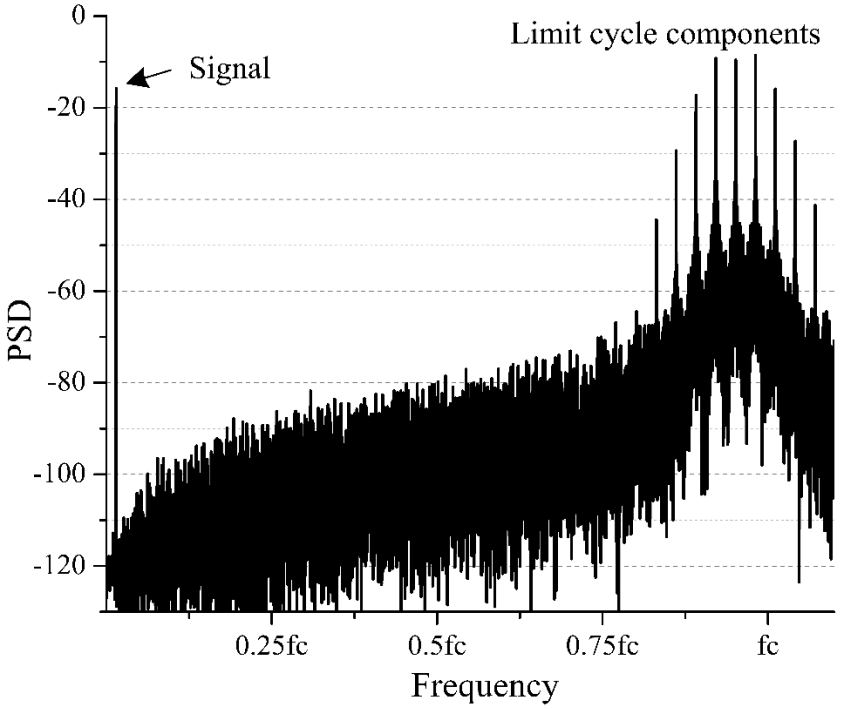


Figure 0-9: Limit cycle frequency components with a small input signal ($V = 0.3$)

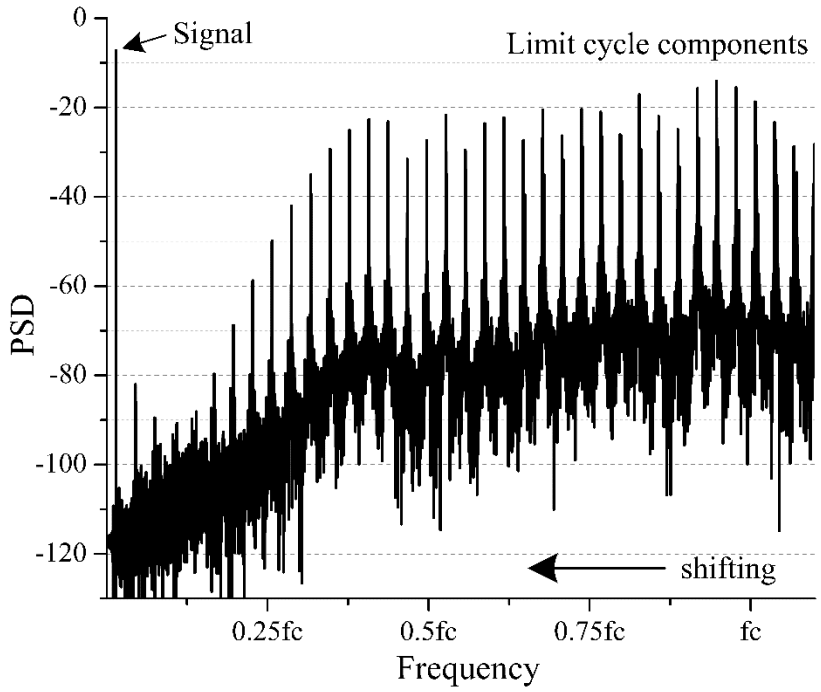


Figure 0-10: Limit cycle frequency components with a large input signal ($V = 0.8$)

1.7.2 Noise performance

Since the input signal amplitude is continuously encoded into the time domain without loss of information, asynchronous sigma delta modulators can be considered as an infinite sampling frequency version of the conventional synchronous sigma delta modulators. Moreover, as there is no quantiser in the system, asynchronous sigma delta modulators do not suffer of quantisation errors. Hence, the signal-to-noise ratio (SNR) in theory can be very high even for a first-order system. This result can be extended to a slowly varying input signal ($f_c / f_{in} >> 1$), and the signal will be only corrupted by harmonic distortion. According to eq. (2-22), we represent the relationship as:

$$V\cos\mu t - (2\alpha - 1) = -\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\sin 2\alpha n\pi}{n}\cdot\frac{\mathrm{Re}\,F(n\omega_0)}{\mathrm{Re}\,F(\mu)} \tag{2-23}$$

The distortion occurs mainly in the right hand section in equation above. Therefore, assuming $\omega_0 = \omega_c\left(1-V^2\right) << \mu$, for an ideal integrator (eq. (2-19)), by inserting $2\alpha = 1+V\cos\mu t$, the right hand section of eq. (2-23) can be rewritten as:

$$\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\sin 2\alpha n\pi}{n}\cdot\frac{\mathrm{Re}\,F\left(n\omega_0\right)}{\mathrm{Re}\,F\left(\mu\right)} \approx \frac{2}{\pi}\sum_{n=1}^{\infty}\left(-1\right)^n\frac{\sin Vn\pi}{n}\cdot\frac{\mu^2}{{\omega_0}^2} \tag{2-24}$$

After a Taylor expansion of $\sin x$ (appendix I), eq. (2-24) becomes:

$$2\alpha - 1 \approx V\cos\mu t + \frac{1}{6}V\frac{\mu^2}{{\omega_0}^2}\cos\mu t + \frac{\pi^2}{6}V^3\frac{\mu^2}{{\omega_0}^2}\left(\frac{3}{4}\cos\mu t + \frac{1}{4}\cos 3\mu t\right) \tag{2-25}$$

The most significant distortion term, the third order harmonic distortion, is:

$$\Delta_3 = \frac{\pi^2\mu^2}{24{\omega_0}^2}V^2 = \frac{\pi^2}{24}\cdot\left(\frac{\mu}{\omega_c}\right)^2\cdot\frac{V^2}{1-V^2} \tag{2-26}$$

While in practice, the pole of the loop filter is non-zero. For first order loop filter:

$$F\left(\omega\right) = \frac{a}{j\omega + p_1} \tag{2-27}$$

Eq. 2-26 can be rewritten as:

$$\Delta_3 = \frac{\pi^2}{24}\cdot\frac{\mu^2 + {p_1}^2}{{\omega_0}^2 + {p_1}^2}V^2 \tag{2-28}$$

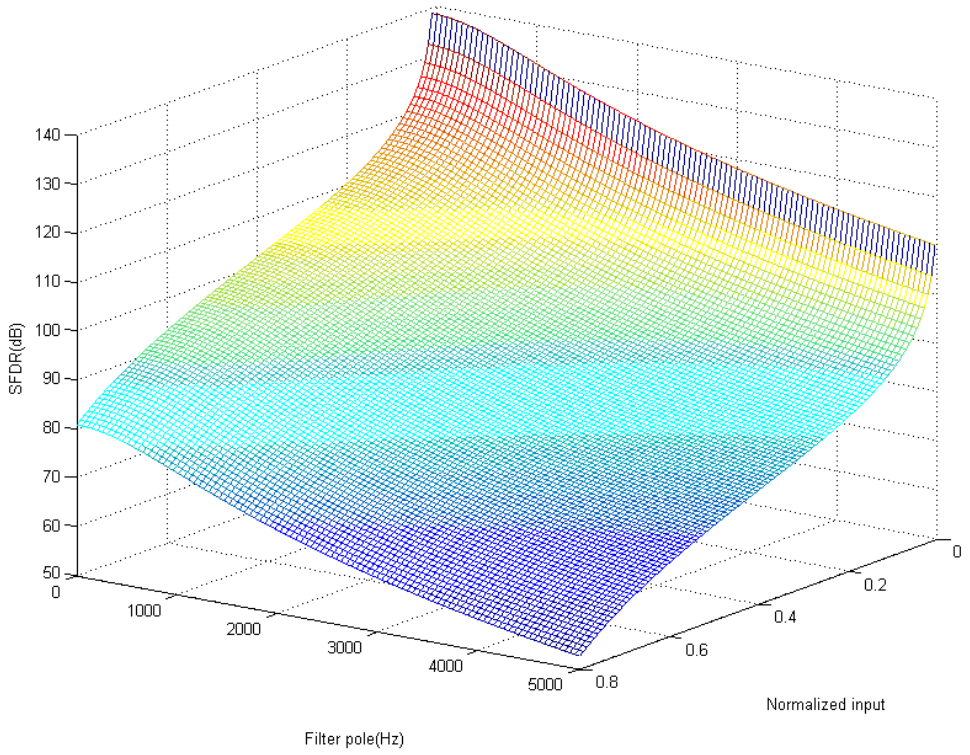


Figure 0-11: Estimation for SFDR of ASDMs versus filter pole and normalized input voltage ($B = 3kHz$, $f_c = 200kHz$)

Fig. 2-11 shows an estimate of SFDR of ASDMs versus signal bandwidth and filter pole. The limit cycle frequency of the modulator is set to 200kHz, and input signal bandwidth is 3kHz. As expected, the pole location of the loop filter will affect SFDR of the modulator. Note that the SFDR of modulators drops approximately 20dB when the pole of the loop filter is equal to the signal bandwidth. In order to minimize this effect, the pole of the loop filter should be set close to the zero.

If we consider a second order loop system:

$$F(\omega) = \frac{a(j\omega + z_1)}{(j\omega + p_1)\cdot(j\omega + p_2)} \tag{2-29}$$

The third harmonic distortion can be rewritten as:

$$\Delta_3 = \frac{\pi^2}{24}\cdot\frac{\mathrm{Re}\,F(\omega_0)}{\mathrm{Re}\,F(\mu)}V^2 \approx \frac{\pi^2}{24}\cdot\frac{\left(\mu^2+p_1^{\,2}\right)\left(\mu^2+p_2^{\,2}\right)}{\left(\omega_0^{\,2}+p_1^{\,2}\right)\left(\omega_0^{\,2}+p_2^{\,2}\right)}\cdot\frac{\omega_0^{\,2}}{\mu^2}V^2 \approx \frac{\pi^2}{24}\cdot\frac{\mu^2}{\omega_0^{\,2}}V^2 \qquad (2\text{-}30)$$

Where $\omega_0 = \frac{p_1 p_2 \pi}{2bz_1}\cdot\frac{V^2}{1-V^2}$, $p_1, p_2 << \mu << \omega_0$

According to eq. (2-29), increasing the order of the loop filter will only slightly improve the SFDR of the modulator. This is quite different from synchronous sigma delta modulators, where a high order loop filter increases drastically the noise shaping performance. The SFDR versus filter pole frequency for second-order loop filter with a double pole ($p_1 = p_2$) is shown in Fig. 2-12. Although the higher order loop filter has a slightly better performance than the first order loop filter for an ideal double integrator (the pole at zero frequency), the high order system is in practice more sensitive to the location of the pole. For the poles at 5kHz, the SFDR of the second order modulator drops to 25dB from 82dB. For the first order modulation, the SFDR reduces to 52dB down from 81dB.

We conclude that performance with first order loop filter is better than with higher order filters, as the first order loop is less sensitive to the filter poles. As long as the limit cycle frequency is sufficiently higher than the signal bandwidth, a first order loop filter suffices for an asynchronous sigma delta modulator to achieve a high SFDR. This will also much simplify the circuit of asynchronous sigma delta modulators than that of synchronous ones. This implies that asynchronous sigma delta modulators have great potential in both low power and high frequency applications.

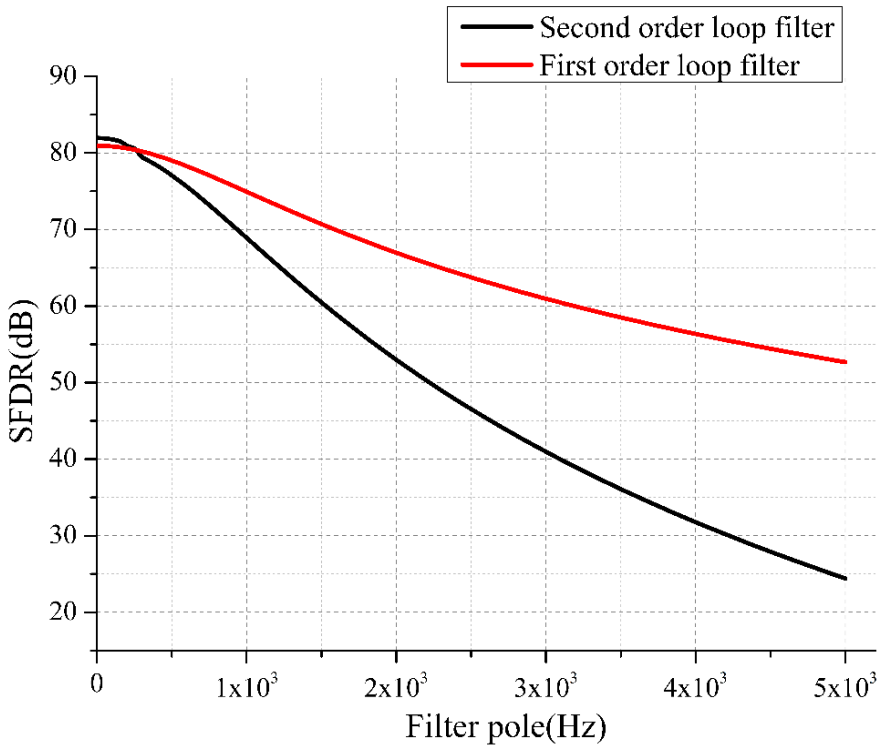


Figure 0-12: Comparison of SFDR between the first order and second loop filters versus pole location ($B = 3kHz$, $V = 0.8$, $f_c = 200kHz$)

A simulation of the achievable spurious free dynamic range (SFDR) of the first order ASDM with normalized input voltage of 0.8 is shown in Fig.2-13. The pole of the loop filter is set to 1kHz. The horizontal axis is the carrier-to-bandwidth ratio, which is the ratio between the limit cycle frequency and the signal bandwidth. This ratio is in a sense similar with the oversampling ratio in synchronous sigma delta modulators; it determines the minimal limit cycle frequency required for a certain conversion accuracy. For example, in order to obtain a SFDR of 75dB for a signal bandwidth of 1kHz with a first order modulator, the limit cycle frequency has to be at greater than 32kHz.

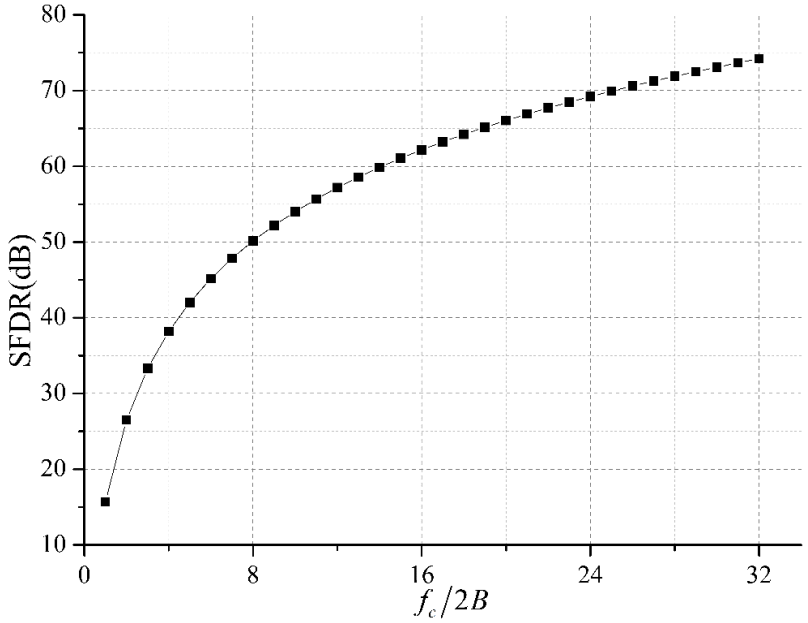


Figure 0-13: Estimation for the achievable SFDR of the first order ASDM ($V = 0.8$, $f_{in} = B/3$, $p_1 = 1kHz$)

1.7.3 Propagation delay

Similar with the conventional synchronous continuous time sigma delta modulators, propagation delay is also an issue in asynchronous sigma delta modulators. In this section, the analysis of the propagation delay is presented.

An asynchronous sigma delta modulator can be modelled as in Fig. 2-14 The propagation delay can be considered as a time shift, which in s-domain is modelled as a multiplicative factor of $e^{\Delta\tau s}$. Similar with the system analysis presented earlier, the effect of the propagation delay will be analysed in two conditions: DC and single frequency sinusoidal inputs.

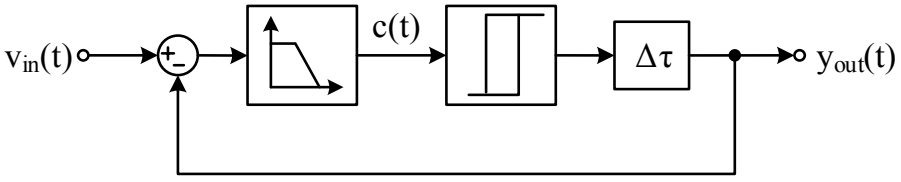


Figure 0-14: System diagram of an asynchronous sigma delta modulator with propagation delay

1.7.3.1 DC input signal

The propagation delay in the system results in an overshoot of the output of the loop filter. This increases the effective value of hysteresis. In Fig. 2-15 the timing diagram is shown with a DC input signal applied. And the positive and negative time intervals are:

$$T_1[n] = \frac{T_c}{2} \cdot \frac{1}{1-V} + \Delta t_1[n] + \Delta t_2[n] \tag{2-31}$$

$$T_2[n] = \frac{T_c}{2} \cdot \frac{1}{1+V} + \Delta t_3[n] + \Delta t_4[n] \tag{2-32}$$

Where $\Delta t_1[n]$, $\Delta t_2[n]$ and $\Delta t_3[n]$, $\Delta t_4[n]$ are the overshoot time in the positive and negative time intervals respectively.

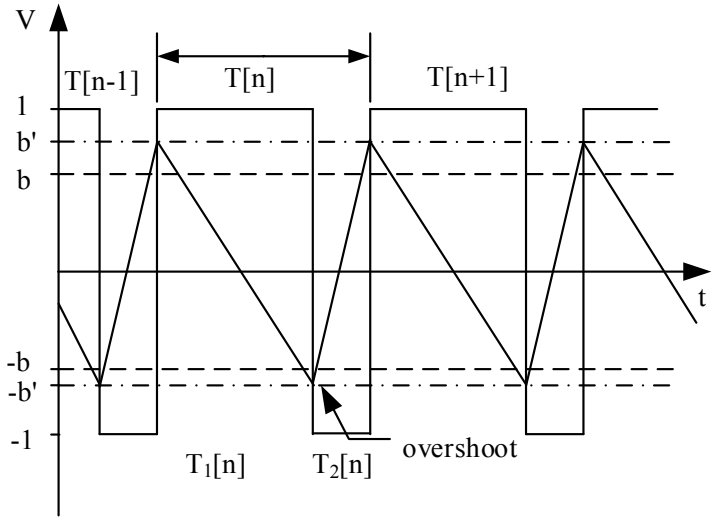


Figure 0-15: Time diagram of asynchronous sigma delta modulators with propagation delay

The overshot of the loop filter is:

$$\begin{cases} b_1 = k_n \Delta\tau + b \\ b_2 = k_p \Delta\tau + b \end{cases} \tag{2-33}$$

Where $k_p = 1-V$, $k_p = 1+V$

Hence the relationship between delay times in each time interval can be shown to be:

$$\Delta t_3[n] = \frac{k_p[n]}{k_n[n]}\Delta t_2[n] = \frac{1-V}{1+V}\Delta t_2[n] \tag{2-34}$$

$$\Delta t_4[n] = \frac{k_p[n]}{k_n[n+1]}\Delta t_1[n+1] = \frac{1-V}{1+V}\Delta t_1[n] \tag{2-35}$$

Where $\Delta t_1[n] = \Delta t_1[n+1] = \Delta t_1$.

In this case the output instantaneous frequency of the modulator becomes:

$$T_0 = \frac{T_c}{2}\cdot\frac{2}{(1+V)\cdot(1-V)} + \Delta t_2[n]\frac{2}{1+V} + \Delta t_1[n]\frac{2}{1+V} \tag{2-36}$$

When the input is zero, the limit cycle frequency becomes:

$$f_c' = \frac{1}{4(b+\Delta\tau)} \tag{2-37}$$

Where $b+\Delta\tau$ is the effective value of the hysteresis.

Note that the propagation loop delay results in a decrease of the limit cycle frequency. Fig. 2-16 the variation of the limit cycle frequency versus the propagation loop delay is shown. When the ratio of $\Delta\tau/T_c$ increases to 0.1, the limit cycle frequency reduces to $0.72f_c$. This issue will become critical in communication applications, such as bluetooth, WIFI, WiMax and CDMA. This is because the maximum limit cycle frequency is bound by the propagation loop delay, which is equal to $1/4\Delta\tau$. This imposes a limitation on the signal bandwidth. The maximum limit cycle frequency reported now right is 250MHz with a signal bandwidth of 8MHz.

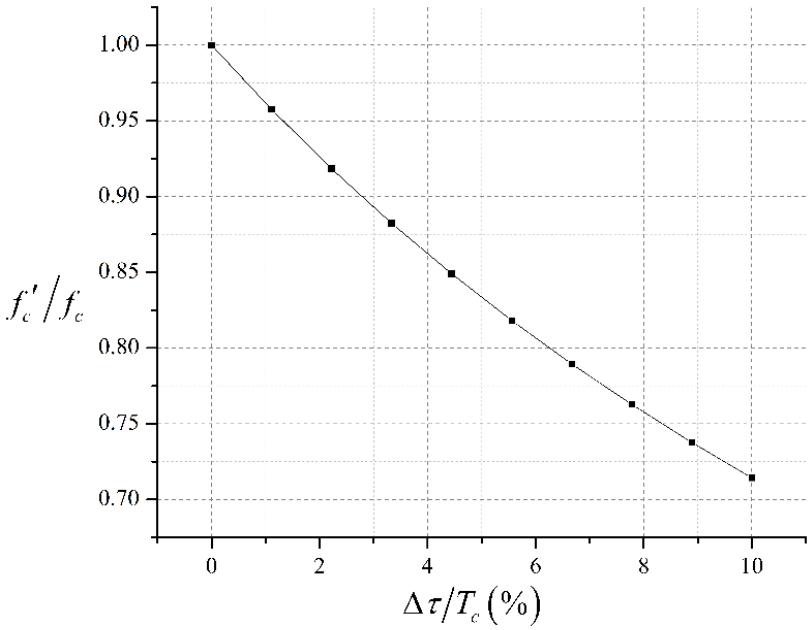


Figure 0-16: Variation of the limit cycle frequency versus the propagation loop delay

According to Fig. 2-15, the duty cycle of the output waveform can be easily derived as:

$$\alpha=\frac{T_1[n]}{T_c}=\frac{\frac{T_c}{2}\cdot\frac{1}{1-V}+\Delta t_1[n]+\Delta t_2[n]}{\frac{T_c}{2}\cdot\frac{2}{(1+V)\cdot(1-V)}+\Delta t_2[n]\frac{2}{1+V}+\Delta t_1[n]\frac{2}{1+V}}=\frac{1+V}{2} \tag{2-38}$$

Here we assume that the propagation delay in the loop is constant. Note that for a DC input signal V , the propagation delay will not affect the duty cycle of asynchronous sigma delta modulators.

1.7.3.2 The sinusoidal input signal

For a sinusoidal input signal eq. (2-13) can be rewritten as:

$$\left[v_{in}-y(t-\Delta\tau)\right]\otimes f(t)=c(t) \tag{2-39}$$

Using the convolution theorem (Appendix II), the following equations can be obtained:

$$\begin{cases} \left[V\cos\mu T_m-(2\alpha-1)\right]\mathrm{Re}\,F(\mu)=\dfrac{2\sqrt{2}}{\pi}\displaystyle\sum_{n=1}^{\infty}(-1)^n\dfrac{\sin 2\alpha n\pi}{n}\mathrm{Re}\,F(n\omega_0)\sin\left(2\pi\dfrac{\Delta\tau}{T_0}+\dfrac{\pi}{4}\right) \\ \qquad\qquad +a\dfrac{\Delta\tau}{T_c}V\cos\mu T_m \\ \displaystyle\sum_{n=1}^{\infty}\dfrac{\sin^2\alpha n\pi}{n}\mathrm{Im}\,F(n\omega_0)\sin\left(2\pi\dfrac{\Delta\tau}{T_0}+\dfrac{\pi}{4}\right)=-\dfrac{\pi\left(b+a\dfrac{\Delta\tau}{T_c}\right)}{4\sqrt{2}} \end{cases} \tag{2-40}$$

Where $a=\dfrac{4}{A_0\cdot b}$.

Note that the propagation loop delay introduces a bias drift to the modulator, which has the same shape and phase of the input signal as shown in Fig. 2-17.

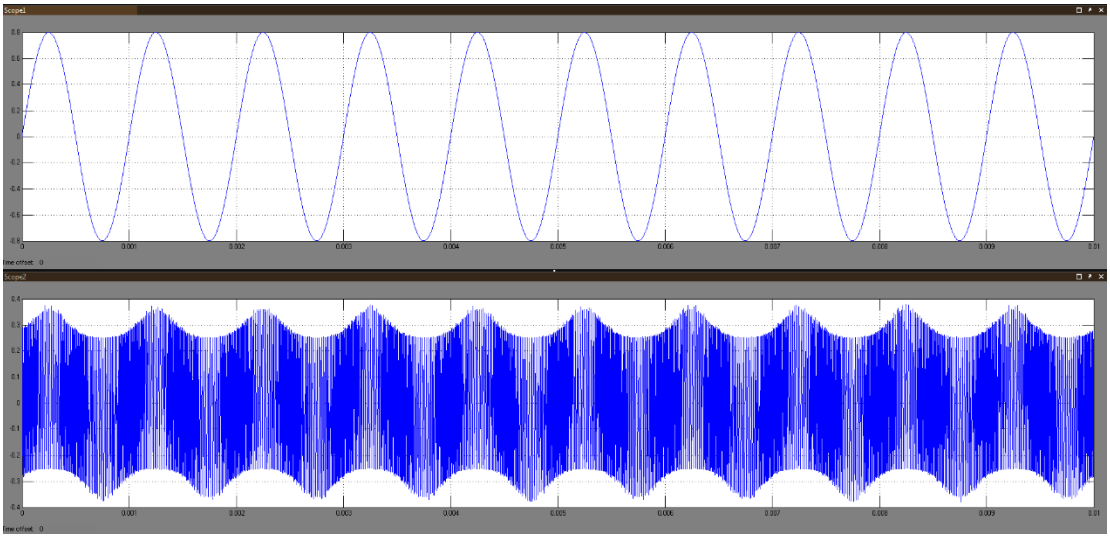


Figure 0-17: Phenomenon of propagation delay

For an ideal integrator, the third order harmonic distortion can be derived as:

$$\Delta_3=\frac{\sqrt{2}\pi\mu^2}{24\omega_0^{\,2}}\sin\left(2\pi\frac{\Delta\tau}{T_0}+\frac{\pi}{4}\right) \tag{2-41}$$

Compared with eq. (2-27), the propagation loop delay results in the distortion function a factor $\sqrt{2}\sin\left(2\pi\frac{\Delta\tau}{T_0}+\frac{\pi}{4}\right)$. The SFDR versus the propagation loop delay is shown in Fig. 2-18. Note that $0.1T_c$ will result in a 8.5dB decrease in SFDR. It can therefore be concluded that the propagation loop delay limits the limit cycle frequency of asynchronous sigma delta modulators, which in turn limits the signal bandwidth if the SFDR of the system is maintained to a certain level. For example, for a 40ps loop delay, the limit cycle frequency will be limited to 250MHz in order to maintain the value of $\Delta\tau/T_c$ within 1%.

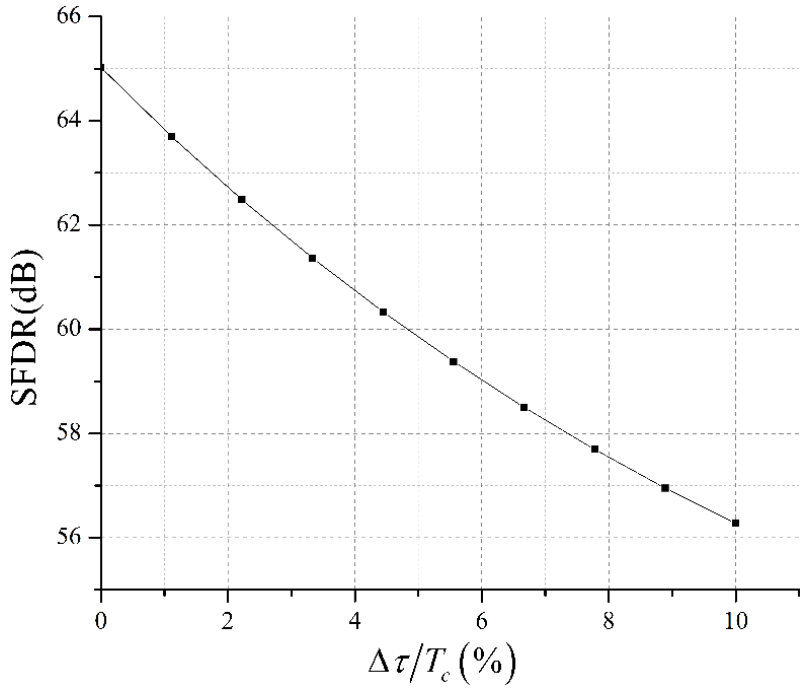


Figure 0-18: SFDR of asynchronous sigma delta modulators with propagation loop delay

1.7.4 The state-of-art of asynchronous sigma delta modulators

Asynchronous sigma delta modulators were first proposed in 1975. Very few publications have appeared over nearly 35 years (Fig. 2-19). This is because synchronous sigma delta modulators were very robust with the effect of oversampling and noise shaping. However, the conventional signal delta modulator is reaching its limits of acceptable power consumption and the maximum speed supported by CMOS technology. During the last 10 years, asynchronous sigma delta modulators have been increasing explored as a potential solution of the problems associated with

sigma delta modulators. The first reported CMOS asynchronous sigma delta modulator was made by S. Ouzounov in Philips Corp. [47]. This modulator was designed for communication applications. It employed a first order loop filter, and achieved a SFDR of 72dB with a signal bandwidth of 8MHz. The central limit cycle frequency was set to 140MHz. In 2006, S. Ouzounov designed another two asynchronous sigma delta modulators which used first order and a second order loop filters respectively [49]. The SFDR of the first order system was 75dB with a signal bandwidth of 8MHz. The second order system, exhibited a SFDR of 72dB over the same signal bandwidth. The only difference between these two integrated circuits was that the central limit cycle frequency of the second order system was 120MHz, while that of the first order system was 140MHz. As demonstrated earlier, increasing the order of the loop filter did not greatly improve the modulator performance. As a matter of fact, it increased the modulator power consumption. In [52], the author used an XOR gate to convert the asynchronous sigma delta modulator to a frequency-to-voltage converter, which could be used as an analogue squarer. In [53], the author presented a special configuration of the asynchronous sigma delta modulator with multiple comparators in paralleled each having a different value of hysteresis. The function of this multi-parallel comparators was similar to that of the multi-bit quantiser in synchronous sigma delta modulators. In theory, doubling the number of comparators should result in a 6dB increase in the modulator performance. However, the main drawback of this configuration is that a complex multi-channel decoding circuit is required, and the mismatch caused by process variation will undermine the performance achieved by this configuration.

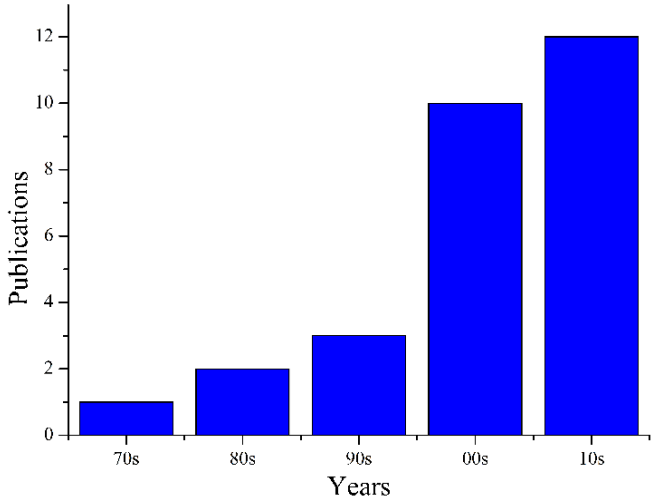


Figure 0-19: Publications of ASDM during 40 years

A drawback of asynchronous sigma delta modulators, relative to synchronous ones is the absence of noise shaping. Some author have proposed combining synchronous and asynchronous sigma delta modulators to solve this problem. In [54], a combination modulator was presented, in which a sample clock was inserted to the loop of the asynchronous sigma delta modulator. This way, first order noise shaping was obtained with a first order modulator. This configuration can be extended to high order systems to obtain a high order noise shaping. However, this way has been sacrificed one of the main advantages of asynchronous sigma delta modulators. This kind of modulator belongs to the class of synchronous sigma delta modulators, since a sampling clock is used to synchronize the binary output. More details of trade-offs involved in noise shaping are presented in Chapter 4.

Currently, asynchronous sigma delta modulators are also proposed for ultra-low power applications. In [55], an asynchronous sigma delta modulator was employed as a signal encoding machine in an electroencephalograph (EEG) system. The limit cycle frequency of this modulator was 1kHz.

1.8 Summary

This chapter provided a brief introduction to the fundamental theory of conventional synchronous sigma delta modulators. The classical configuration and important design equations were discussed. A literature review of recent integrated implementations of synchronous sigma delta modulators was also presented. The drawbacks of synchronous sigma delta modulators were introduced. The asynchronous sigma delta modulators were introduced as s solution to the limitations of synchronous modulators. The fundamental system analysis asynchronous sigma delta modulators was presented in detail. The noise performance and important non-ideal effects including harmonic distortion and the effect of loop propagation delay were explained. The fundamental theory presented in this chapter will be frequency referred to and used throughout the dissertation.

The Asynchronous Sigma Delta Modulator with a Novel Time-to-Digital Converter

1.9 Introduction

The analysis of asynchronous sigma delta modulators was presented in Chapter 2. Asynchronous sigma delta modulators have many advantages, including the absence of quantisation errors, and immunity to clock jitter. When this modulator is used for data conversion, the main challenge is how to extract the information from the modulated square wave and how to synchronize to the digital output.

In theory, the signal can be recovered by applying an ideal low pass filter with a cut-off frequency at the signal bandwidth. When asynchronous sigma delta modulators are used in A/D data conversion, a decoding circuit is required. The simplest one is the sample & hold (Fig.3-1). The total noise power P_N within a bandwidth B amounts to [45]

$$P_N = \frac{8}{3} f_0 T_s^2 B \tag{3-1}$$

The signal-to-noise ratio (SNR) of such a modulator can be described by:

$$SNR = \frac{3V^2}{\sqrt{2}\left(1-V^2\right)} \cdot \frac{f_s^2}{f_0^2} \cdot F \tag{3-2}$$

Where $F = f_c / 2B$ is the carrier-to-bandwidth ratio, V is the normalized input amplitude.

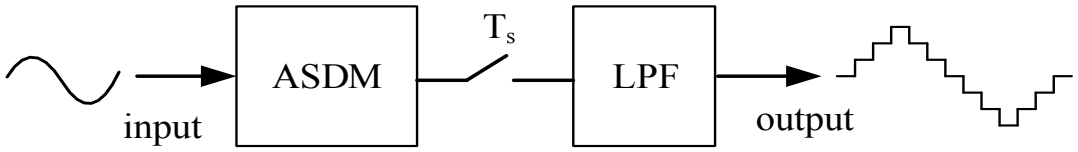


Figure 0-1: System diagram of the ASDM with a sampler

Fig. 3-2 shows an estimate of the achievable SNR versus OSR for several different values of the normalized input amplitude. Note that a very high $f_s/2f_c$ is required to achieve a high SNR with a first order asynchronous sigma delta modulator. Even with an oversampling ratio as high as $f_s/2f_c = 1024$, the SNR is still less than 80dB. This is because of the absence of a feedback loop to shape the quantisation errors.

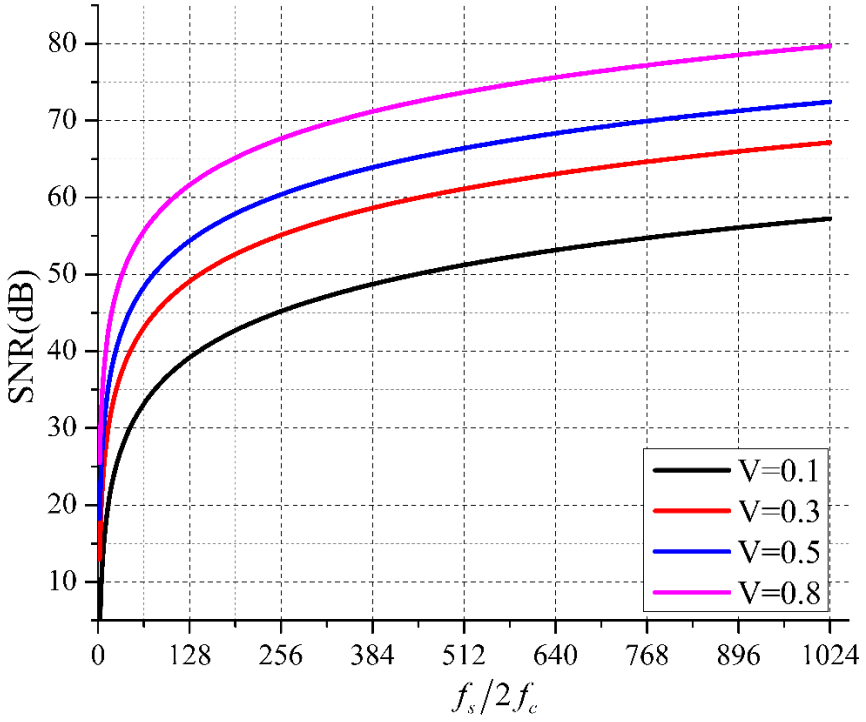


Figure 0-2: Estimation for achieved SNR versus oversampling rate in different input amplitude ($f_c/2B = 32$, $f_{in} = B/3$)

1.10 Time signal processing

In conversional analogue-to-digital converters, the signal resides in the voltage or current domain [56]. The rapidly emerging deep sub-micro-meter CMOS technologies, however, focus on

improving speed, reducing supply voltages, and increasing the packing density of the digital circuits [57]. These pursuits give rise to many challenges for the analogue design in the mixed-signal system design. Firstly, reducing the transistor size dimensions and gate oxide thickness reduces the system operating voltages, which makes the transistors work at non-optimal operating points. This also increases transistor leaking currents. Secondly, a lower voltage power supply results input voltage swing and diminishes the linear range in analogue circuit design. A potential approach to solve these problems, referred to as time-mode signal processing [58] is introduced. The idea of time-mode signal processing is fairly new; its potential in many applications [59-70], especially in data conversion, has been discussed by a number of authors.

Time mode signal processor can be defined as detection, storage, and manipulation of sampled analogue information using time-difference variables [71]. It provides a means to implement analogue signal processing functions in any technology using the most basic element available, i.e., propagation delay. An analogue-to-digital converter based on time-mode signal processing comprise three parts: a voltage-to-time converter, a time quantiser, and sampler & synchronization, as shown in Fig. 3-3. The asynchronous sigma delta modulator can be implemented as the voltage-to-time converter, and the time-to-digital converter is used as a time quantiser to generate the digital format output signal.

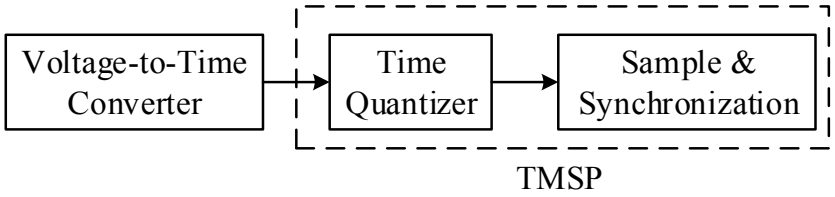


Figure 0-3: System diagram of the analogue-to-digital converter based on TMSP

Time information cannot be sampled, stored, and amplified in the same fashion as an amplitude measurement. The best way to measure time information is to implement a time-to-digital converter. There are many types of time-to-digital converters; they can be divided into two types: analogue and digital. Analogue time-to-digital converters (TDC) convert time information to amplitude first; this can be easily realized by an ideal integrator, such as a constant current charge pump and a capacitor. This solution is also known as stretch interpolation [72]. This method is not

suitable here, as it requires another analogue-to-digital converter for the final digitization, implying a significant silicon overhead and design complication. The digital method depends on synchronously counting clock cycles of a reference oscillator. Evidently, the resolution of such a converter is expressed in terms of the frequency of the reference clock. This kind of the time-to-digital converter can be realized with D flip-flops and other digital blocks, which will be scribbled as follows.

3.2.1 Coarse counting

The simplest time-to-digital converter is used a counter, as shown in Fig. 3-4. In this converter, the input time interval is measured by a high resolution counter, which is driven by a reference clock, of frequency f_s or period $T_s = 1/f_s$. The resolution (LSB) of this circuit depends on the reference clock equals to T_s. The maximum quantisation error of a single measurement usually limited to ± 1 clock cycle, depends on the true value of the time interval and its location with regards to the reference clock. The on-chip reference clock constrains the circuit performance in high resolution and low power consumption applications.

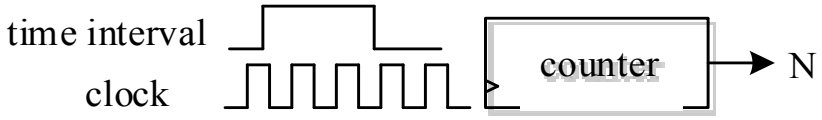


Figure 0-4: Counter as a simple time-to-digital converter

3.2.2 Flash time-to-digital converter

Flash time-to-digital converters are analogous to flash analogue-to-digital converters for voltage amplitude encoding and operate by comparing a signal edge to a number of reference edges all displaced in time [73]. The input signal is compared to the reference usually with flip-flops or arbiters. In the single delay chain flash time-to-digital converter shown in Fig. 3-5, the resolution is limited by the delay through a single gate in the semiconductor technology used. A drawback of this implementation is that in order to achieve a large dynamic range, a large number of delay elements is required, which will significantly increase time jitter. Moreover, a long delay chain

will suffer mismatches caused by temperature dependencies and process variation. A delay locked loop (DLL) can be employed to stabilize the accuracy of the delay chain [74].

The main advantage of flash time-to-digital converters is the ability to perform a measurement on every reference clock period. In other words, they are suitable for high resolution measurement, such as clock jitter measurement [75]. Flash time-to-digital converters can be realized in any standard CMOS process, and also on general purpose devices including FPGAs [76].

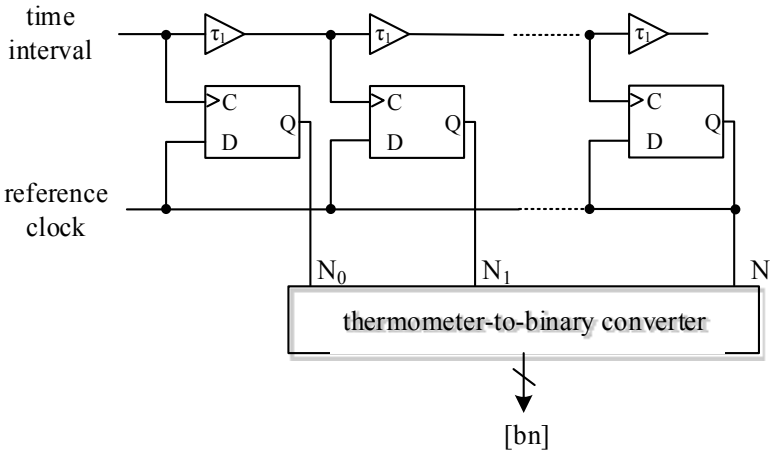


Figure 0-5: Configuration of the flash time-to-digital converter

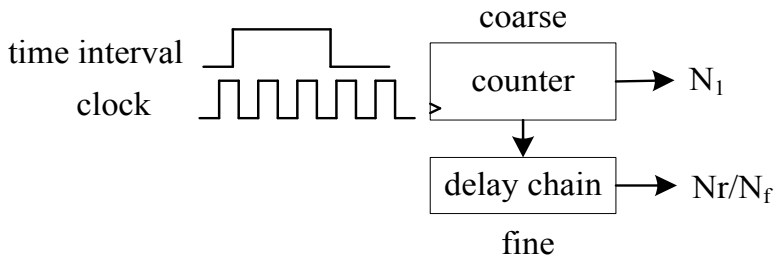
3.2.3 Coarse-fine time-to-digital converter

Coarse-fine time-to-digital converters separate the measurement process into two parts: a coarse measurement and a fine measurement. They are similar to sub-ranging analogue-to-digital converter. A coarse time measurement can easily be made with a coarse counter, limited by the IC technology used, with a time resolution on the order of approximately 1ns. The fine measurement can be realized by many methods developed to perform sub-nanosecond time interpolation. For example, delay interpolation can be used to subdivide the reference clock period into small even-sized time samples.

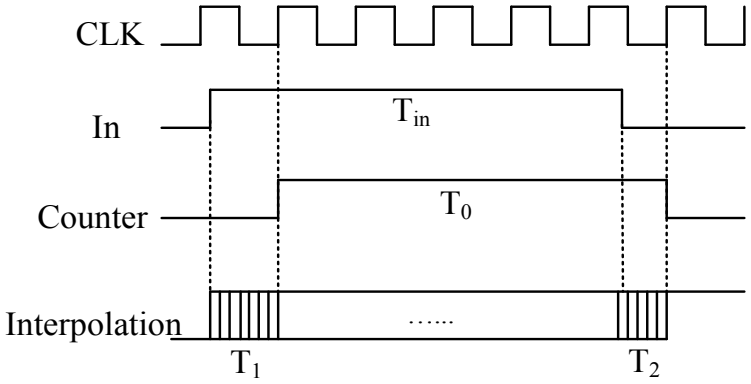
Fig. 3-6 shows the basic architecture of a coarse-fine time-to-digital converter. The input timing signal can be described as:

$$T_{in} = T_0 + T_1 - T_2 = N_1 T_{ref} + \left(N_f - R_r\right)\Delta t \tag{3-3}$$

Where N_r and N_f is the interpolated results of the start phase and the stop phase respectively, Δt is the resolution of the delay line, N_1 is the counter result value, and T_{ref} is the reference clock period.



(a)



(b)

Figure 0-6: (a) System diagram of the coarse-fine time-to-digital converter; (b) Timing diagram of the converter

The main advantage of coarse-fine time-to-digital converters is that the number of the digital components is significantly reduced, since the dynamic range of the fine measurement is only one period of the reference clock. Coarse-time time-to-digital converters can achieve a sub-gate-delay resolution by implementing multi-interpolation technology. In [62], a two-step delay line interpolation time-to-digital converter, which realizes the 10ps resolution, is presented. The drawback of this kind of coarse-time time-to-digital converter is that measurement speed is limited, since a conversion requires $N_1 + n$ clock cycles.

3.2.4 Cyclic pulse-shrinking time-to-digital converter

A time-to-digital converter can be realized through the application or pulse-shrinking circuit in a feedback loop, as shown in Fig. 3-7 [77]. This is equivalent to a "time attenuator". An input pulse of width W_{in} is compressed in time as it propagates around the feedback loop by some scale factor α; eventually, the pulse-width disappears. As the rising edge of the pulse reaches a counter, a count is made until the pulse disappears undetectable. The inverter chain is used to set the feedback delay to be longer than the pulse duration, so that the pulse-shrinking element operates on only one signal at a time [71].

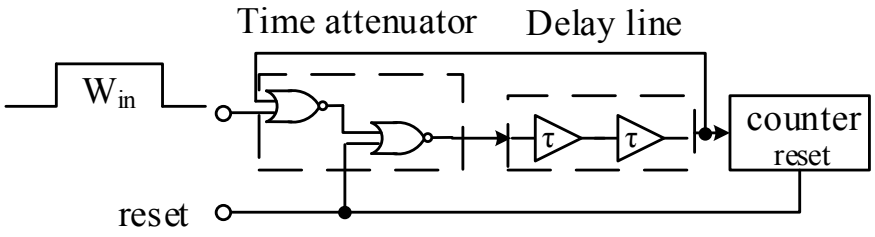


Figure 0-7: Block diagram of the cyclic pulse-shrinking TDC [77]

The system behaviour can be written as:

$$W_{out}\left[n\right] = \alpha W_{out}\left[n-1\right] \tag{3-4}$$

The general solution of eq. (3-4):

$$W_{out}\left[n\right] = \alpha^{n} W_{in} \tag{3-5}$$

The output counter is incremented until the final pulse-width is smaller than the hold time of the counter; the final counter value will be a representative of the input pulse-width. The main drawback of the cyclic pulse-shrinking time-to-digital converters is that a long conversion time is required for one measurement.

1.11 Time-to-digital converter using vernier delay lines

The relationship of the input signal amplitude and the output square wave can be rewritten as:

$$V_{in} = \frac{T_1 - T_2}{T_1 + T_2} \tag{3-6}$$

The conventional method to decode the output signal of the asynchronous sigma delta modulator is to implement a time-to-digital converter to locate the positive of the time intervals. Assuming that the output frequency is constant (equivalent to assuming that the input is small), the input signal can be easily reconstructed:

$$V_{in} = \frac{N_1 - N_2}{N_0} = \frac{N_1 - N_2}{N_1 + N_2} \tag{3-7}$$

Where $T_1 = N_1 \Delta t$, $T_2 = N_2 \Delta t$, N_0 is constant, and it is equal to the dynamic range of the time-to-digital converter.

The converter resolution is:

$$\Delta V = \frac{(N_1 + 1) - (N_2 - 1)}{N_0} = \frac{2}{N_0} \tag{3-8}$$

However, because of the ASDM's phase modulation characteristic, the output frequency will decrease, when the input signal increases. Consequently, the error of the solution above will significant increase. For instance, when the normalized input voltage is 0.8, the output frequency will reduce to $f_0 = 0.36 f_c$, which is almost one third of the limit cycle frequency. One way to solve this problem is to increase the dynamic range of the time-do-digital converter by a factor of three relative to the initial one, which will significantly increase the complex of the system. A novel solution to this issue is presented here, which measures the time intervals T_1 and T_2 asynchronously.

1.11.1 System level design

In order to measure the duty cycle directly, the conventional solution is to implement two separate time-to-digital converters. This approach doubles the chip area and power dissipation. We propose a novel structure, which measures the duty cycle with one time-to-digital converter. The principle of the proposed decoding scheme is to make the duty cycle measurement independent of the period of the data signal. Therefore the proposed decoding scheme can obtain the duty cycle without measuring the instantaneous period of the data signal.

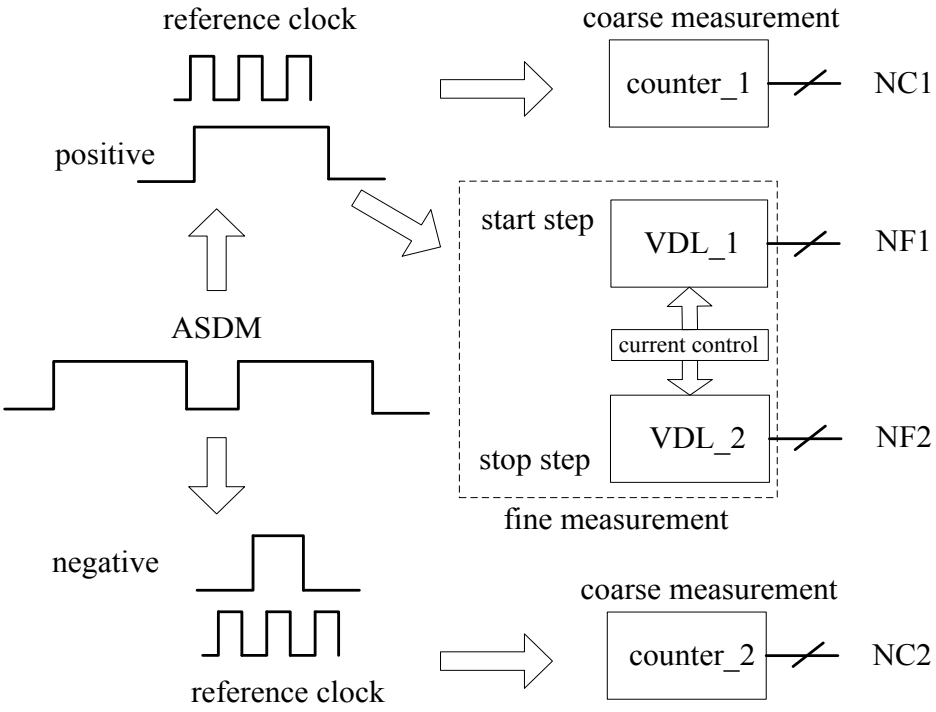


Figure 0-8: System diagram of the proposed ASDM decoding circuit

The system diagram of the proposed time-to-digital converter is shown in Fig. 3-8. The proposed circuit's operation is based on the coarse-fine measurement. Two counters are used for the coarse measurement. The fine measurement, on the other hand, is performed by two vernier delay lines. Firstly, the input data signal is separated into two time intervals, and each one will be measured by a counter with a reference clock. The vernier delay lines determine the location of the rising and falling edges of the time intervals in one period of the reference clock, so as to reduce the quantisation errors.

Fig. 3-9 shows the timing diagram of the proposed circuit. The time intervals $T_1[n]$ and $T_2[n]$ can be described as:

$$\begin{cases} T_1[n] = NC_1[n]T_{ref} + \left(NF_1[n] - NF_2[n]\right)\tau_0 \\ T_2[n] = NC_2[n]T_{ref} + \left(NF_2[n] - NF_1[n+1]\right)\tau_0 \end{cases} \tag{3-9}$$

Here T_{ref} is the period of the reference clock; τ_0 is the resolution of the vernier delay line; NC_1 and NC_2 are the output of the two coarse counters; NF_1 and NF_2 are the output of the vernier delay lines.

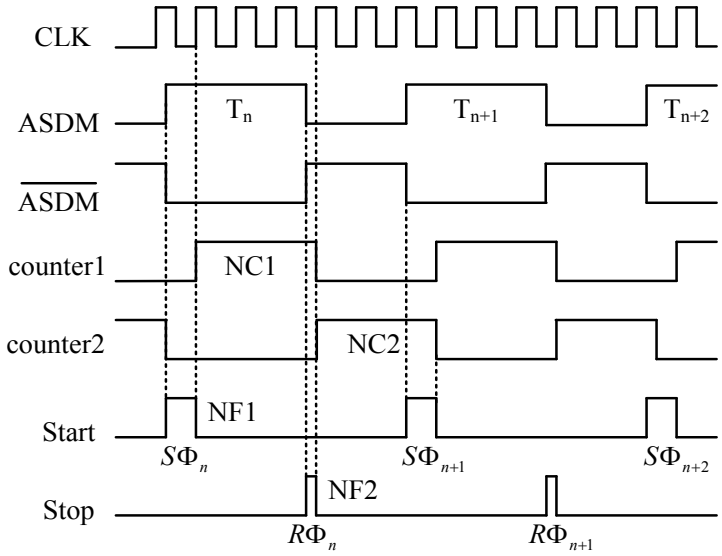


Figure 0-9: Timing diagram of the proposed circuit

The period of the data signal can be, therefore written as:

$$T[n] = T_1[n] + T_2[n] = \left(NC_1[n] + NC_2[n]\right)T_{ref} + \left(NF_1[n] - NF_1[n+1]\right)\tau_0 \tag{3-10}$$

It is interesting to observe that the period of the data signal can be measured without additional time-to-digital converter. In other word, the proposed decoding scheme can measure the duty cycle

of the data signal without the period of the data signal, which perfectly solve the frequency variation issue.

1.11.2 Vernier delay lines

The fine measurement vernier delay line (Fig. 3-10) consists of two slightly different delay buffer chains W_1 and W_2. The elements of the two delay chains have delays τ_1 and τ_2 ($\tau_1 > \tau_2$) respectively. The start and stop signals represent the events whose time difference is to be measured, and are propagated on the W_1 and W_2 lines. The time difference $t_m = t_{stop} - t_{start}$ decreases by $\tau_0 = \tau_1 - \tau_2$ after each stage of the vernier delay line. After N_x stages, the start signal will catch up with the stop signal. The N_x position comparator will signal a logical "1" to stop measurement. The vernier delay line output contains a thermometer coded value of $N_x = t_m \bmod \tau_0$. The final measurement is constrained:

$$N_x \tau_0 < t < (N_x + 1)\tau_0 \tag{3-11}$$

Since the resolution of vernier delay lines is no longer based on the delay time τ_1 and τ_2, high resolution can be achieved with a low frequency clock. While a low reference clock will increase the measurement time.

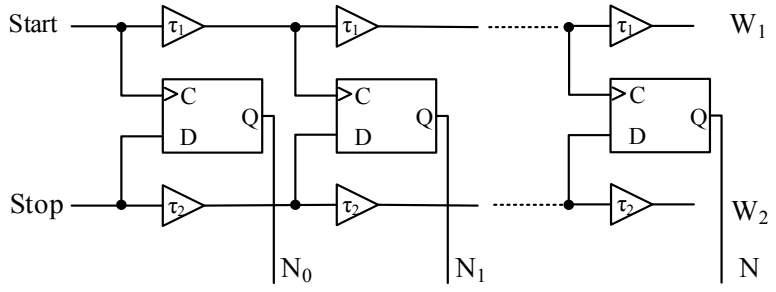


Figure 0-10: Basic configuration of the vernier delay line

There is a critical disadvantage of the vernier delay line. The dynamic range of an *N*-stage vernier delay line utilizing delay chains τ_1 and τ_2 is

$$T_{DR} = N\tau_R \tag{3-12}$$

While the maximum propagation delay of the vernier delay line is

$$T_{Max} = N\tau_1 \tag{3-13}$$

Note that the T_{Max} is slightly larger than T_{DR}. This, of course, means that the reset time of the vernier delay line is larger than its measurement time. Two measurements will overlap, since a measurement event can start to propagate in the delay line while the previous one is still propagating. P. Dudek used an extra read-out pipe to solve this problem [78], where the results stored in the D flip-flops are read out before the next measurement coming.

While this is not an issue with the proposed asynchronous converter. Fig. 3-11 shows one slice of the proposed vernier delay lines. Two D flip-flops in series are used here and they are triggered by the rising edge of the input time interval. The first D flip-flop, which is similar as that in basic vernier delay lines, serves to measure the location of the time interval in one period of the reference clock. The other one read out the result in the previous one, and feeds it into the thermometer-to-binary decoder. The maximum transfer speed is the limit cycle frequency of the asynchronous sigma delta modulator. In order to avoid overlapping, each vernier delay line measurement should finish before the arrival of the next trigger event. The worst case occurs when the output frequency is equal to the limit cycle frequency f_c, and meanwhile the fine measurement also reaches the dynamic range. In this case, the time interval is $T_{in} = 1/2f_c$, and the measured time for each delay line is:

$$T_m = N \cdot \tau_1 < N \cdot \tau_0 + \frac{T_c}{2} = \left(1 + 2^{n-1}\right) \cdot T_{ref} \tag{3-14}$$

Here T_{ref} is the reference clock in the counter, $n > 0$ is the number of bits of the counter and N is the output of the vernier delay line.

Note that overlapping can be avoided if we ensure that the delay of each delay line in the vernier delay lines is smaller than the minimum time interval $\left(1+2^{n-1}\right)T_{ref}$.

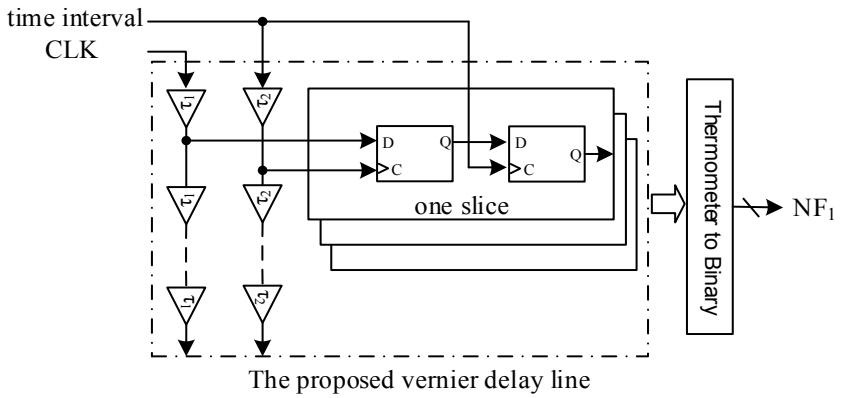


Figure 0-11: Configuration of the proposed vernier delay line (each slice is one stage of the delay chains)

We rewrite the duty cycle of the modulator:

$$\alpha[n]=\frac{NC_1[n]+\tau_0\left(NF_1[n]-NF_2[n]\right)}{N_0\tau_0\left(NC_1[n]+NC_2[n]\right)+\tau_0\left(NF_1[n]+NF_1[n+1]\right)} \tag{3-15}$$

Where $N_0=T_{ref}/\tau_0$ is the number of stages of a delay line which fits in one period of the reference clock.

In practical design, the reference clock frequency and the number of bits of the counter must be selected according to the specified range of time measurements. On the one hand, the counter cannot expire before the end of the longest time interval is measured, which means f_{ref} cannot be too high. On the other hand, this frequency also should be not so slow that the measurement may miss the minimum time interval of the modulation. According to eq. (2-10), the minimum time interval at the output of asynchronous sigma delta modulator is:

$$T(\min)=\frac{T_c}{2}\cdot\frac{1}{1\pm V}\geq\frac{T_c}{4} \tag{3-16}$$

Consequently, the frequency of the reference clock and the number of bits of the counter should meet the following conditions:

$$\begin{cases} 2^n T_{ref} \geq \dfrac{T_c}{4\left(1-V_{\max}\right)} & 0<V<1 \\ T_{ref} \leq \dfrac{T_c}{4} \end{cases} \tag{3-17}$$

In practice the modulator will overload when the normalized input amplitude V exceeds the value of 0.8. The dynamic range of the measurement then is:

$$T_{DR} = T\left(\max\right) - T\left(\min\right) = \frac{2V}{1-V^2}\frac{T_c}{4} \leq 2^n T_{ref} \tag{3-18}$$

Note that the minimum number of bits of the counter is 4, when the frequency of the reference is set to be $f_{ref} = 4f_c$.

1.11.3 Noise performance

As there is no time quantisation in the asynchronous sigma delta modulator, the signal-to-noise ratio of the modulator mainly depends on the time-to-digital converter resolution. The minimum input amplitude, according to eq. (3-15), is:

$$\Delta V = \frac{2\tau_0}{T_c} = \frac{2\tau_0}{2^{n-2}T_{ref}} = \frac{1}{N_0 2^{n-3}} \tag{3-19}$$

Here we assume the variation of the output frequency is very small. The signal-to-noise ratio is given by the well know quantisation noise expression:

$$SNR = 6.02\left(n-2\right)+1.76+20\log_{10}\left(VN_0\right) \tag{3-20}$$

Fig. 3-12 shows an estimate of signal-to-noise ratio of the ASDM with time-to-digital converter versus length of the vernier delay lines in different numbers of bits of the counter. The SNR can increase by 6dB either by increasing the counter with by one bit or by doubling the length of the vernier delay line.

Fig. 3-13 shows the SNDR of the ASDM with proposed TDC, where the resolution of the TDC is 10ns. When the normalized input amplitude is small ($V \le 0.1$), the harmonic distortion is smaller than the noise introduced by the time-to-digital converter. The SNDR is increased when the carrier-to-bandwidth ratio $f_c/2B$ is increased. On the other hand, if the input signal amplitude is very large ($V = 0.8$), the maximum SNDR is obtained when a low carrier-to-bandwidth ratio is given.

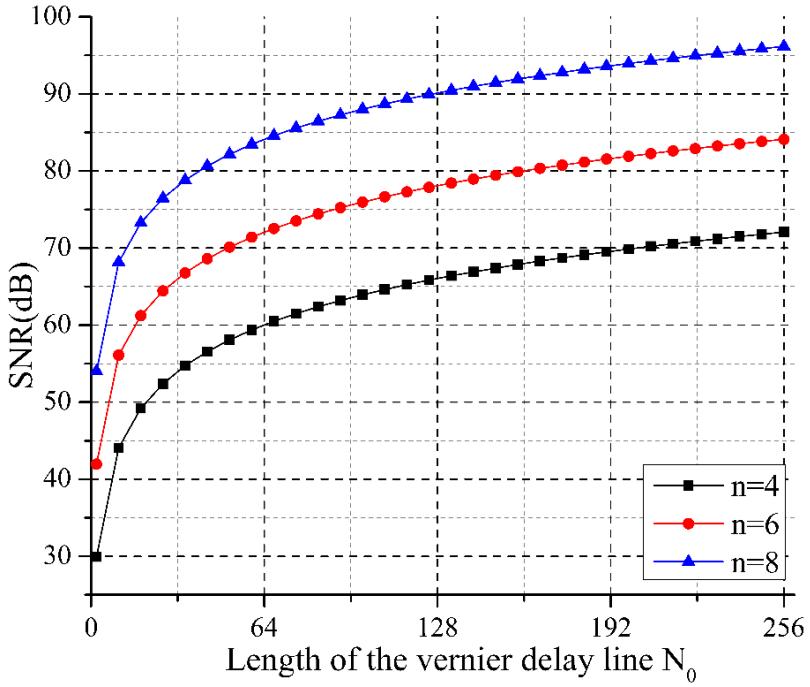


Figure 0-12: Estimate of the achievable SNR of ASDM with the TDC for different numbers of bits of the counter

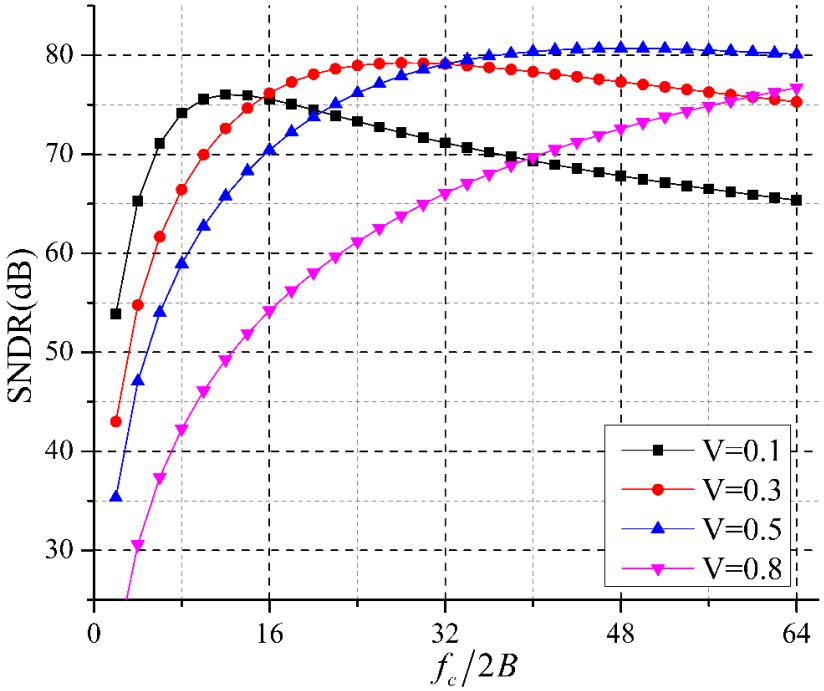


Figure 0-13: Relationship between $f_c/2B$ and SNDR in different modulation index ($f_{in}=B/3$, $f_s=10MHz$ $p_0=2kHz$, $B=3kHz$ and $\tau_{res}=10ns$)

1.11.4 Demodulation algorithm

Measuring time intervals of the modulated square wave is only the first step of the decoding process. In order to finish the reconstruction of the original signal, the output of the time-to-digital converter must be synchronized to the sampling clock f_s , then down sampled to the Nyquist frequency rate ($f_N=2B$) and finally interpolated by a digital low-pass filter. This conversion is not straightforward.

The demodulation process for a conventional time-to-digital converter is illustrated in Fig. 3-14. The demodulation algorithm is:

$$V[kT_s]=\frac{T_1[kT_s]-T_2[kT_s]}{T_1[kT_s]+T_2[kT_s]} \tag{3-22}$$

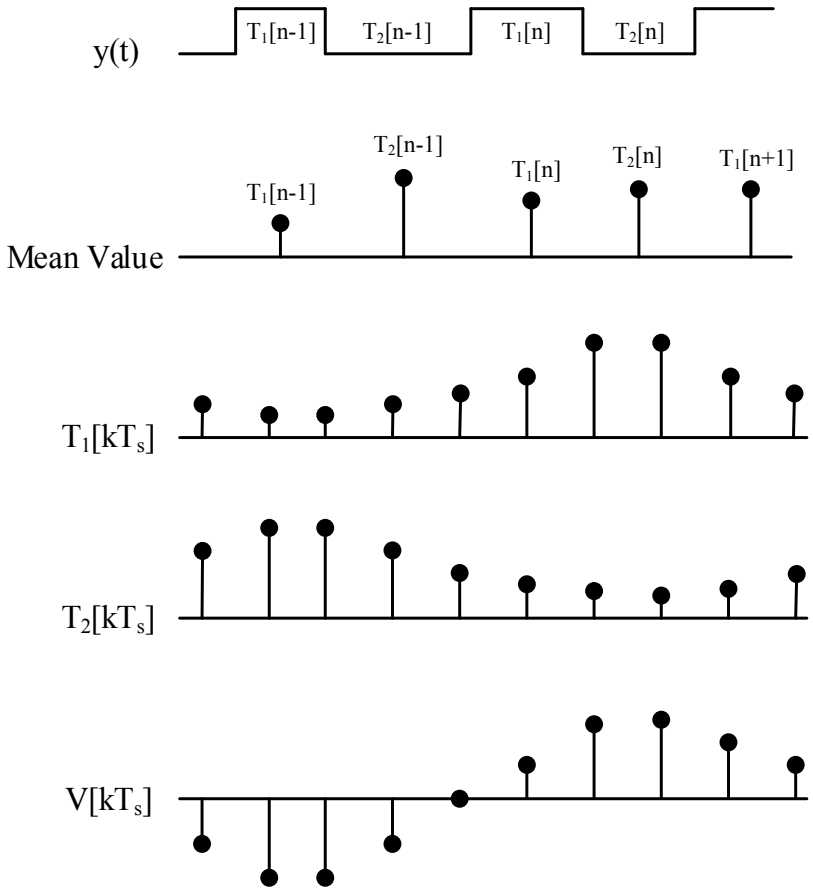


Figure 0-14: Illustration of the demodulation for the conventional TDC

As the conventional TDC only locates the position of the time intervals, the challenge is to accurately estimate the values of $T_1[kT_s]$ and $T_2[kT_s]$. According to [79], a high frequency sampling clock is required to minimize the quantisation errors.

While the demodulation with the proposed time-to-digital converter is quite different form the conventional one, because the proposed TDC measures time intervals directly. The output of the TDC is quantised value of time intervals, and it do not require an extra high frequency clock to re-quantise. The operation of the proposed TDC is shown in Fig. 3-15. In the demodulation process, first step is to synchronize the asynchronous output signals to the reference clock.

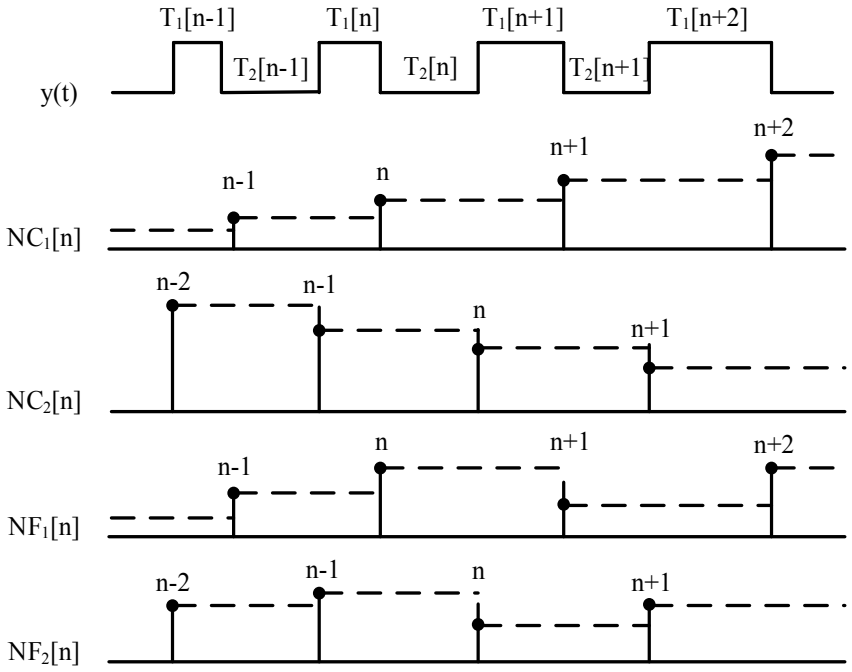


Figure 0-15: Operation of the proposed coarse-fine TDC

The synchronization block is shown in Fig. 3-16. Firstly, the output of the proposed time-to-digital converter needs to be synchronized to the reference clock. In Fig. 3-16, the measurement of $NC_2[n]$ and $NF_2[n]$ are slightly delayed, because their registers are triggered by the $n+1$ th period of $y(t)$. D flip-flops are used to shift the measurement of $NC_1[n]$ and $NF_1[n]$ to synchronize all the nth measurement to the rising edge of the $n+1$ period of $y(t)$. In the synchronization block, two consecutive flip-flops reduce the chance of a metastable output. Therefore, the demodulator output is given by:

$$V[kT_s] = \frac{T_1[kT_s] - T_2[kT_s]}{T[kT_s]} \tag{3-25}$$

$T_1[kT_s]$, $T_2[kT_s]$ and $T[kT_s]$ can be easily obtained though eq. (3-9) and (3-10). No additional is required to demodulate the output of the proposed time-to-digital converter.

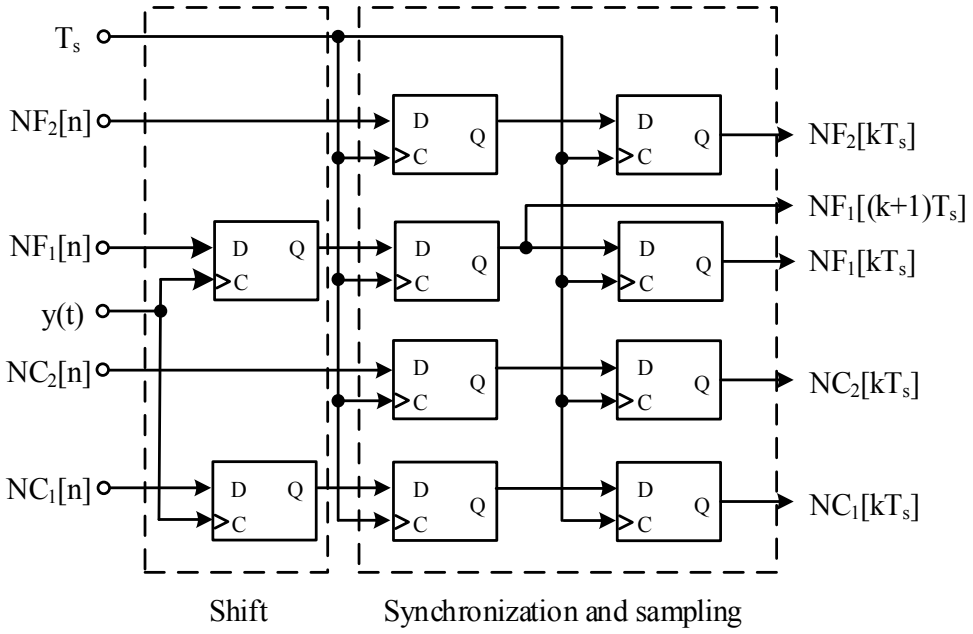


Figure 0-16: Configuration of the proposed synchronizer

1.11.5 Limitations

The main drawback of the ASDM with the proposed time-to-digital converter is that it does not perform noise shaping. In order to obtain noise shaping, the proposed configuration must be converted into a closed loop system by the addition of a high resolution digital-to-analogue converter in the feedback path, shown in Fig. 3-17. However, the performance of the noise shaping decreases with increasing input amplitude, as shown in Fig. 3-18. Given that an ideal DAC is used to establish the feedback, the performance will in practice be worse than expected.

In conclusion, the closed-loop system performs much better when a small signal with a wide bandwidth is applied, as is common in communications applications. On the other hand, the open loop system (without noise shaping) performs better with a low limit cycle frequency and a large input. This means that, the open loop system is more suitable in ultra-low power applications.

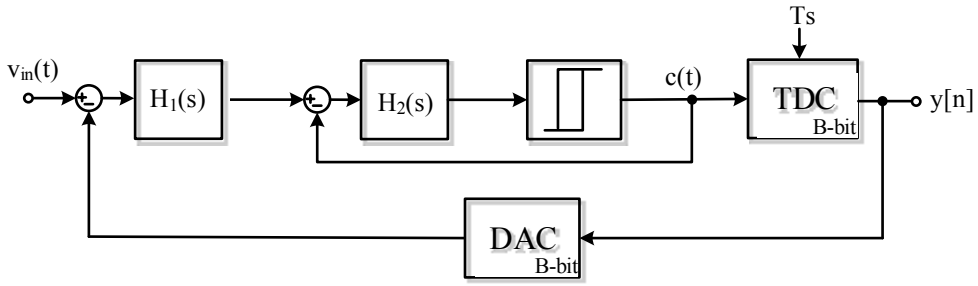


Figure 0-17: Configuration of the ASDM with noise shaping

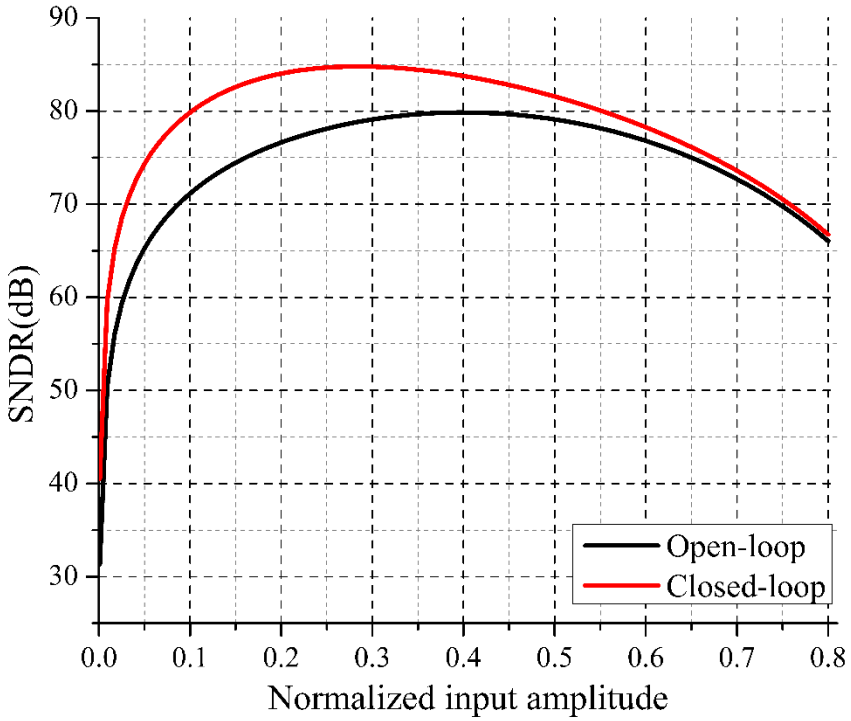


Figure 0-18: Relationship between SNDR and modulation index (with the same sample clock)

Noise shaping can also be added by the introduction of a gate-ring oscillator [56]. The disadvantage of this solution is complexity, but also, and in order to minimize errors of the demodulation, a very high sampling clock is required.

1.12 Circuit design

1.12.1 Asynchronous sigma delta modulator

It has been shown that the limit cycle frequency is the main design specification for the asynchronous sigma delta modulator. A suitable carrier-to-bandwidth ratio is required to obtain a high performance. As an illustration design example $f_c/2B = 32$ was chosen. f_c is determined by the loop filter properties, the hysteresis value in the comparator:

$$f_c = \frac{kV_{fb}}{4b} \tag{3-26}$$

Here b is the hysteresis value, $k = 1/RC$ is the integration gain of the loop filter and V_{bf} is the feedback voltage amplitude.

The system can be divided into several blocks: the loop filter, the comparator and feedback.

1.12.1.1 Loop filter design

A continuous-time integrator can be realized by many methods, such active RC, switched-capacitor (SC) and transconductance-C (Gm-C). It is conventionally accepted that active RC filters achieve better linearity, because of the use of a high open loop gain amplifier [80]. Typical third harmonic distortion levels are around -80dB. However, in closed-loop operation, the bandwidth is typically limited to a few MHz. The benefit of high open loop gain is limited at a small bandwidth. Active RC filters are notorious for sensitivity to component variation of passive resistors and capacitors. Resistors often need to be individually trimmed after fabrication. Switched capacitor implementations overcome the mismatch problem of the RC filters because the filter parameters depend on capacitor ratios which can be controlled accurately in standard CMOS processes. In the present application controlling clocks are not desirable, as we aim to realize a clock-free modulator-converter. Gm-C filters are reputed to achieve wideband operation form several hundred of kHz to more than 100MHz [81]. However, they suffer with the poor linearity because of their open-loop operation.

Considering the target limit cycle frequency, the configuration of the loop filter, shown in Fig. 3-19 is chosen. The loop filter is operated in the full differential mode in order to minimize second order harmonic distortion. Its transfer function is:

$$H(s) = \frac{g_{m1}}{sC_{\text{int}}} \tag{3-28}$$

Therefore, eq. (3-27) can be rewritten as:

$$f_c = \frac{V_{fb} g_{m1}}{4bC_{\text{int}}} \tag{3-29}$$

Note that the first Gm-cell affects the limit cycle frequency.

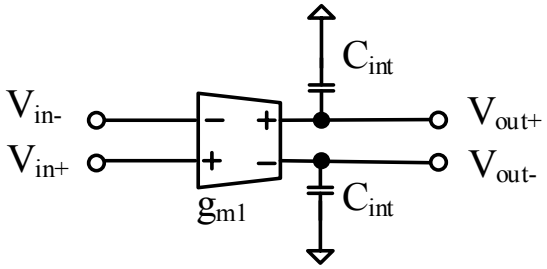


Figure 0-19: Configuration of the Gm-C integrator

The challenge in designing Gm-C filters is to realize a wide input dynamic range with high linearity. The quality of the loop filter implementation determines the quality of the conversion in the baseband, with respect to SNDR. In order to achieve SNDR of the modulator over 60dB (10-bit resolution), the loop filter must have a least 60dB linearity with a full range input. Several techniques have been developed to minimize the distortion, including as source degeneration, cross-coupling and active biasing. The basic principle is to use negative feedback to minimize the distortion by which increasing power consumption. In the proposed implementation, a $3\mu A/V$ fully differential OTA is required. The configuration of the OTA is shown in Fig. 3-20.

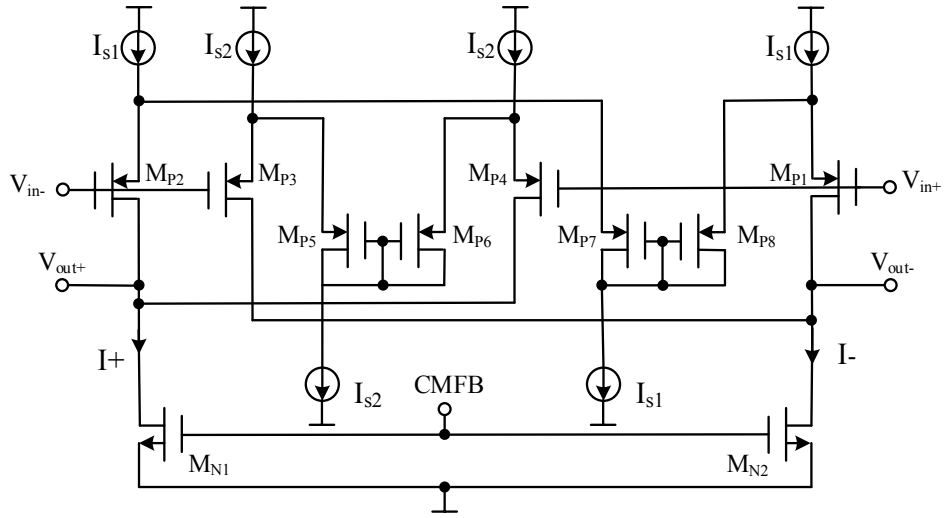


Figure 0-20: Configuration of the proposed OTA

Transistors M_{P1} ~M_{P4} form a cross-coupled pair. The principle of this configuration is to cross couple two differential pairs to cancel out both even and odd order harmonics of distortion. The 3rd order harmonic distortion (HD_3) is:

$$HD_3 = \frac{k_n^{2/3}}{2\sqrt{2I_s}} V_{id}^{3} \tag{3-27}$$

Where $k_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$, V_{id} is the differential input voltage and I_s is the DC bias current.

Since HD_3 only depends on the ratio of $k_n^{3/2}$ and $I_s^{1/2}$, the distortion can be cancelled by connecting two differential pairs in parallel with the same distortion. The size of transistors $M_{P1,2}$ and $M_{P3,4}$ are related to I_{s1} and I_{s2} as follows:

$$\left(\frac{k_{p3,4}}{k_{p1,2}}\right)^3 = \frac{I_{s2}}{I_{s1}} \tag{3-28}$$

The ratio of I_{s1} and I_{s2} must be optimized. When $I_{s2} << I_{s1}$, non-linearity cancellation is reduced, while power consumption due to I_{s2} decreases. As I_{s2} approaches I_{s1}, the variation of effective transconductance reduces. However, the gain and output swing of the Gm cell also reduce, so that the CMRR of the modulator reduces as well. Moreover, power consumption and noise approximately double. For this implementation, the ratio of I_{s1} and I_{s2} is chosen to be 4.

Another technique implemented here is to add another negative feedback in each differential pair in the form of source degeneration. Since resistors are assumed to be absent, they are done by transistors M_{P5} ~M_{P8}. They function as active loads, saturated resistors with their drain connected to their gate. In this technique, the third-harmonic distortion, which is the most important one, decreases by a factor of n^2, where factor n is determined by the ratio of transconductance between active loads and differential pairs. The transconductance of each differential pair also reduces by the same factor n. In fact, this ratio cannot be very high, where the noise performance and speed will degrade. For the topology in Fig. 3-19, the factor n is set to be 2.

Therefore, the effective transconductance of the proposed OTA can be derived as:

$$g_m{}' = \frac{g_{m1,2}}{n}\left[1-\left(\frac{I_{s2}}{I_{s1}}\right)^{2/3}\right] = 0.3g_{m1,2} \tag{3-29}$$

By cross couples and emitter degeneration, the proposed OTA can achieve a high linear, wide range and small value transconductance. The continuous time common mode feedback in the proposed OTA is realized by a balanced difference amplifier [82]. Being first block of the modulator, the loop filter determines noise performance. For low noise designs, the flicker noise is the major concern. The corner frequency in $0.35\mu m$ standard CMOS process is about 400kHz. PMOS input pairs are chosen because of their lower flicker noise. Another common way to decrease the effect of flicker noise is to increase transistor sizes. The sizes of the transistors are listed in Table 3-1.

Table 0-1: Transistors sizes in the proposed OTA

Transistor	Size(W/L)
M_{P1},M_{P2}	$15\mu m/1\mu m$
M_{P3},M_{P4}	$9\mu m/1\mu m$
M_{P5},M_{P6}	$3\mu m/5\mu m$
M_{P7},M_{P8}	$2\mu m/3\mu m$
M_{N1},M_{N2}	$4\mu m/2\mu m$

Fig. 3-21 shows the simulated transconductance variation of the OTA with input voltage. A flat response (with variation smaller than 0.1%) is obtained over a range of about $\pm 100mV$. The integrating capacitance is chosen to be big enough to mask the influence parasitic at the output node.

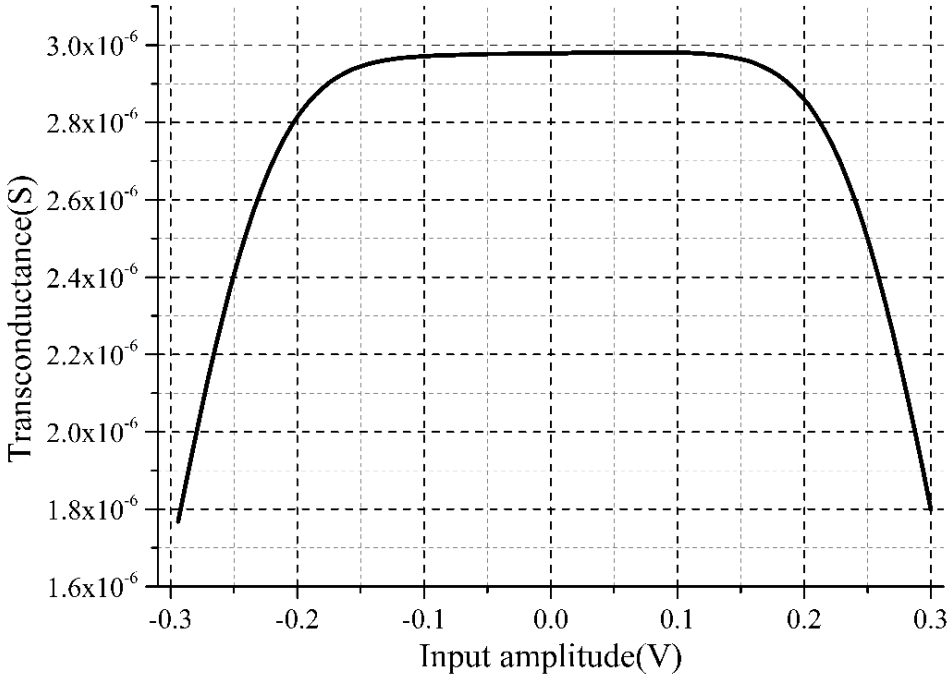


Figure 0-21: Gm of the OTA versus input voltage

1.12.1.2 Comparator with hysteresis

There are many methods to introduce hysteresis in a comparator. The basic principle is the same: hysteresis is obtained by the addition of positive feedback [83]. In order to simplify the circuit and

avoid the use of additional passive components, in this work hysteresis is implemented internally. The schematic of the comparator is shown in Fig. 3-22. In this circuit there are two feedback paths. The first one is current series feedback formed by transistors M_{N1}, M_{N2}, M_{P1} and M_{P2}. This is a negative feedback loop. The other path is the voltage-shunt feedback form by transistors M_{N3} and M_{N4}. This feedback path is positive. Hysteresis will arise when the positive feedback factor is larger than the negative one. The static hysteresis values are given by:

$$b = \sqrt{\frac{2I_{bias}}{k_{n1,2}}}\frac{\sqrt{a}-1}{\sqrt{a+1}} \tag{3-30}$$

Where α is the W/L ratio between M_{N3}, M_{N4} and M_{N1},M_{N2}.

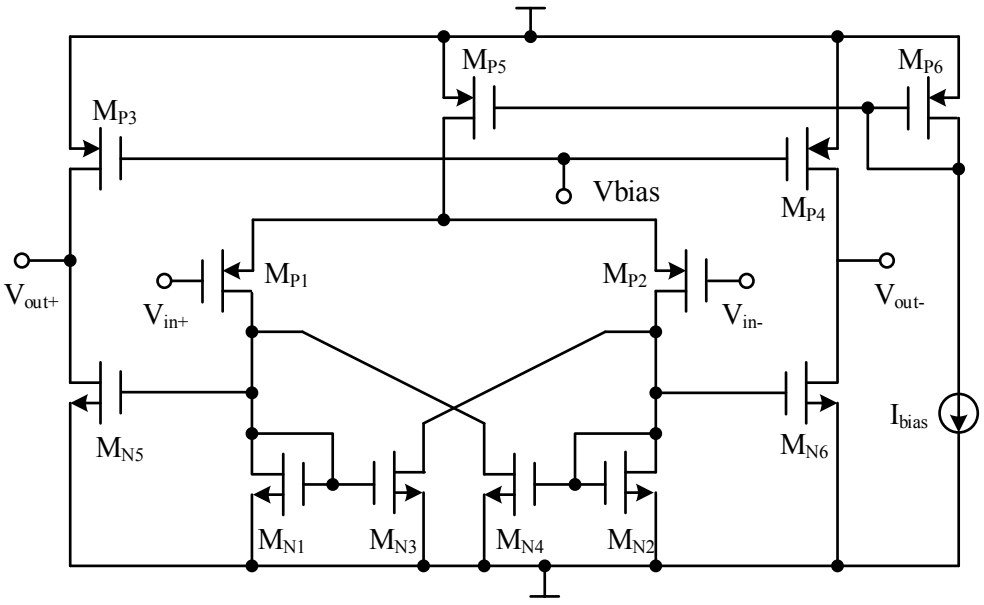


Figure 0-22: Schematic of the comparator with internal hysteresis

In the implementation, the ratio is $\alpha = 2$, and the hysteresis of the comparator is $40mV$. Table 3-2 lists the transistors sizes in the comparator.

Table 0-2: Transistors sizes in the proposed comparator with hysteresis

Transistor	Size(W/L)
M_{P1},M_{P2}	$50\mu m/1\mu m$
M_{P3},M_{P4}	$4\mu m/2\mu m$
M_{P5},M_{P6}	$12\mu m/2\mu m$
M_{N5},M_{N6}	$10\mu m/2\mu m$
M_{N1},M_{N2}	$6\mu m/2\mu m$
M_{N3},M_{N4}	$10\mu m/2\mu m$

1.12.1.3 Feedback

The negative feedback block is shown in Fig. 3-23 [47]. A switched-current source feedback is implemented here, controlled by the output of the modulator directly. Compared with conventional voltage feedback, the switched-current source feedback has two advantages. The first one is avoiding using the voltage divider; the other one is that it will not occupy the linear input dynamic range of the Gm cell, which reduces the design challenge of the OTA and the power dissipation as well. Transistors M_{P1} and M_{P2} are chosen to have large, widths and minimum L so as to minimize their ON resistance. The feedback current, together with the forward current, determine the full range input of the modulator. The relationship between normalized input voltage and the feedback current is:

$$V = \frac{V_{DR}}{g_m I_{feedback}} \tag{3-31}$$

Where V_{DR} is the maximum input range of the loop filter.

A cascade current mirror is used to increase the accuracy of the mirror current, and also to increase the gate source voltage of transistors M_{P1}, M_{P2}.

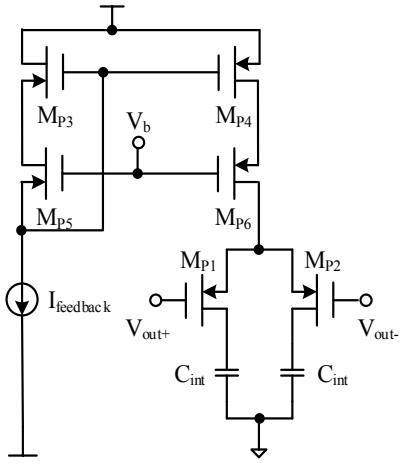


Figure 0-23: Schematic of the feedback block

1.12.1.4 Simulation results

All simulations were performed using the Spectre simulator on the Cadence platform. The PSD of the asynchronous sigma delta modulator described in this chapter is shown in Fig. 3-24. As expected, a SFDR of 71.3dB is obtained. More results are listed in Table 3-3.

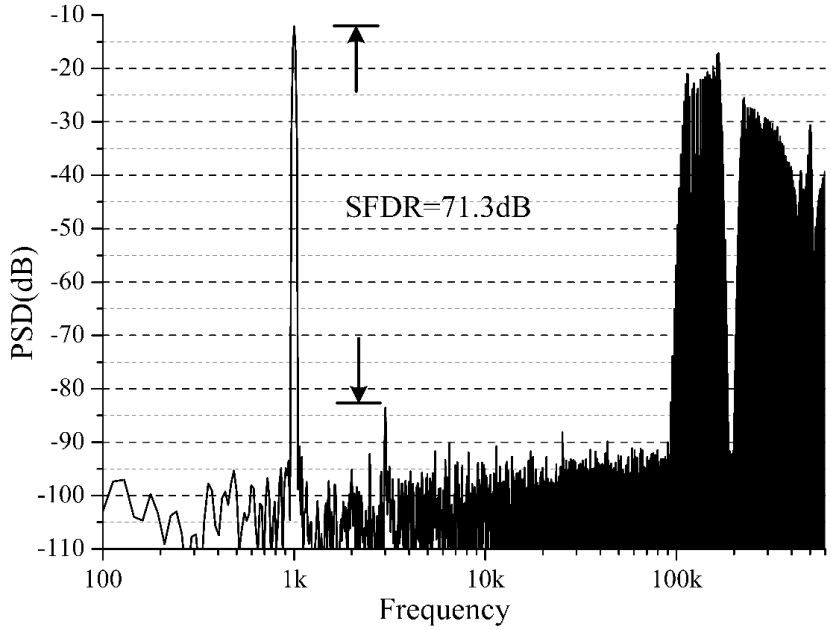


Figure 0-24: PSD of the first order asynchronous sigma delta modulator ($f_{in} = 1kHz$, and $V = 0.8$)

Table 0-3: Simulation results for the ASDM

Parameter	Results
f_c	$200kHz$
Normalized input amplitude (V)	0.8
Bandwidth	$3kHz$
Input range	$\pm 100mV$
SFDR	$71.3dB$
Supply Voltage	$\pm 1V$
Power consumption	$120\mu Watts$

1.12.2 Time-to-digital converter based on vernier delay lines

1.12.2.1 Vernier delay line

As can be seen from Fig. 3-9 in the previous section, this configuration consists of a voltage controlled delay line and time comparators. Details of the delay lines will be given first. Variable delay lines elements fall into either of two categories: digitally-controlled delay elements and voltage-controlled delay elements. The first type is realized by a variable length of delay elements. The magnitude of the delay is determined by number of elements used in the chain. The resolution of the delay chain is determined by the delay time of a single delay element. This kind of delay chain can be easy realized by FPGAs. The second one is more appropriate for applications where small, accurate, and precise value of delay is necessary. This is particularly true when sub-gate delay resolution and ultra-low power of operation are required. Evidently, as there are the design considerations in the realization of vernier delay lines, the analogueue controlled delay elements are a more suitable design choice.

Fig. 3-25 shows the configuration of the voltage controlled delay lines. The delay time is controlled by a control voltage $V_{control}$. There are two types of voltage controlled delay lines. The first one is shunt capacitor, and the other one is current starved. For the shun-capacitor type of delay lines a large value of the output capacitor is required in order to realize a large delay time. This takes up a large silicon area. Moreover, the maximum delay and the range of voltage regulation are both relatively small. The current starving delay line, because of its low power consumption and wide range of voltage regulation, it is suitable for the implementation here. However, it suffers of

fluctuations and large temperature sensitivity. For high resolution implementation, PLLs or DLLs are required.

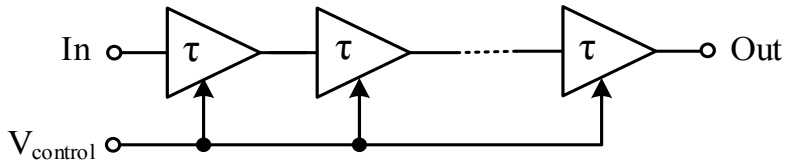


Figure 0-25: Configuration of the voltage controlled delay line

There are two types of voltage controlled current-starved delay elements. The first one is shown in Fig. 3-26. This type of delay elements uses two bias transistors to control the charge/discharge current of two inverters. The advantage of this configuration is it requires the smallest number of transistors, occupies the smallest chip area and has the lowest power consumption. The drawback of this VCDL is that since the current is only starved at the bottom of the inverter, the charging and discharging time are asymmetric. Furthermore, the maximum delay time is limited by the pulse width of the input clock. If the delay time is larger than the pulse width of input clock no signal will propagate to the output of the delay line.

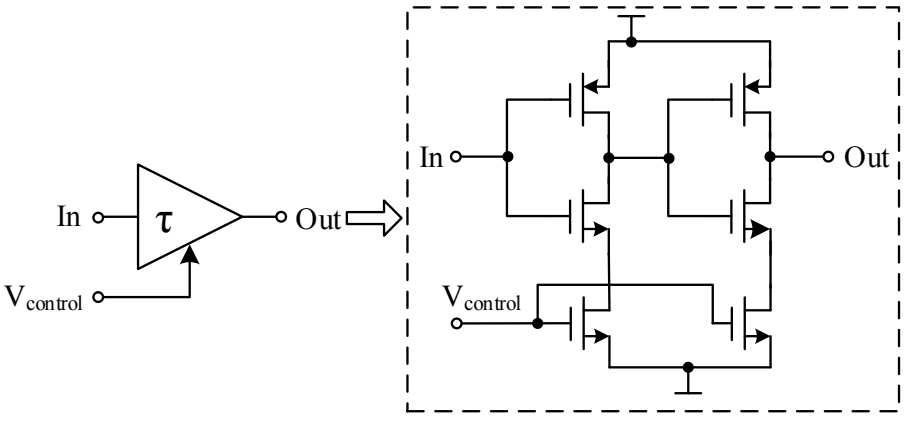


Figure 0-26: Schematic of the asymmetrical voltage controlled delay element

The second type of delay elements uses a symmetric configuration, as shown in Fig. 3-27. This type of delay element requires more transistors than the previous one. As a results, both the power consumption and chip area will increase. Bias transistors are placed in both the top and the bottom of the inverters, so that this type of delay elements is more symmetric between rising and falling

edges of the output signal. The configuration can be simplified to six transistors by removing the bias transistors in the second inverter in order to save chip area. A side effect of this size optimisation is that the power consumption will increase. The drawback of this type of delay elements is that two control voltages are required. This issue can be easily solved by using of current mirrors. This way one control voltage can control both upper and bottom bias transistors.

Considering the chip area, the six transistor configuration was chosen. Furthermore, in order to minimize device mismatch and channel length modulation, bias transistors (current mirrors) need to have a big enough gate length.

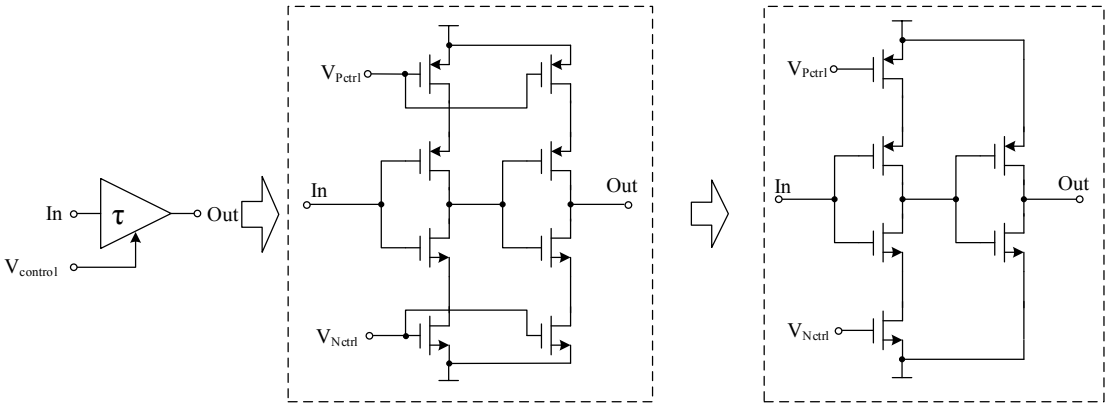


Figure 0-27: Schematic of the symmetric voltage controlled delay element

Delay elements suffer of poor linearity. Fig. 3-28 shows the delay time versus the control voltage. The delay time is inversely proportional to the control voltage:

$$\tau_0 = \frac{V_{sw} C}{I_0} \tag{3-32}$$

Where C is the parasitic output capacitance, I_0 is the charging/discharging current and V_{sw} is the output swing voltage.

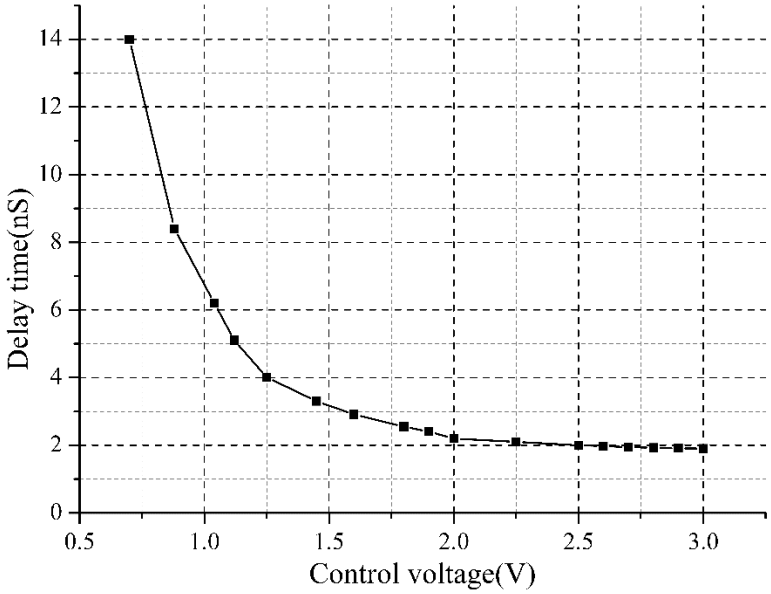


Figure 0-28: Delay time versus the control voltage

A big limitation of the conventional voltage controlled delay line is its poor linear performance. For current starved delay lines, the delay time is inversely proportional to the charge/discharge current, which has a square law dependence on the control voltage. To solve this issue, a translinear loop is implemented here, operated in the current mode. The purpose of this circuit is to generate a current inversely proportional to a control current; by cascading the translinear loop and the current starved delay line, a linear relation between the control current and the delay time is obtained. The configuration of the translinear loop is shown in Fig. 3-29. The relationship between the four transistors' gate voltages is:

$$V_{GS1} - V_{GS2} = V_{GS4} - V_{GS3} \tag{3-33}$$

Assuming that all transistors operate in weak inversion, eq. (3-31) can be rewritten as:

$$I_y = I_1 \times I_2 / I_x \propto 1/I_x \propto \tau_R \tag{3-34}$$

Where $I_1 = I_2 = I_0$ is constant bias current source.

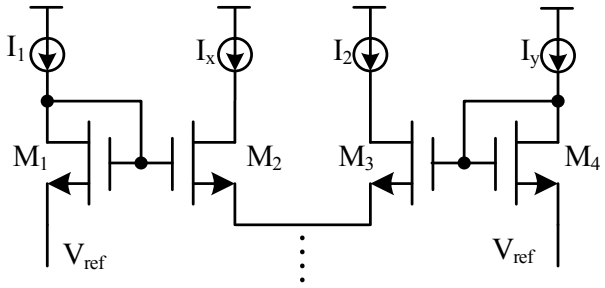


Figure 0-29: Configuration of the translinear loop [84]

By cascading eq. (3-33) and eq. (3-34), a linear control of delay time is achieved:

$$\tau_0 = \frac{V_{sw} C}{I_0^{\,2}} I_x \tag{3-35}$$

Here I_x is the controlled current.

The linear performance of the translinear loop is illustrated in Fig. 3-30, where the residual of the output current is within 1nA from perfect linearity for an input range from 200nA to 300nA.

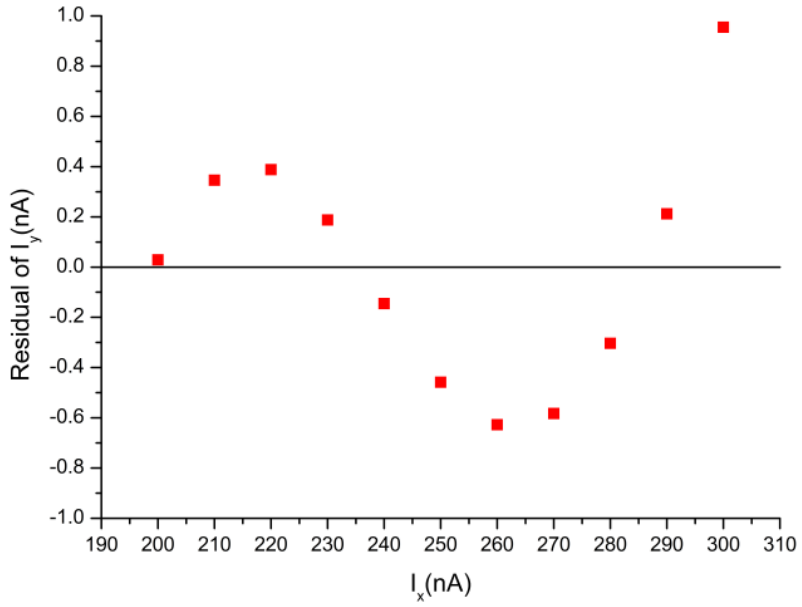


Figure 0-30: Linearity of the translinear loop ($I_0 = 200nA$)

The time comparators can be implemented simply by D flip-flops. Here the TSPC (True Single Phase Clocking) D flip-flop (Fig. 3-31) is used in the vernier delay line in order to improve the to time measurement. Transistor sizing is critical for achieving the correct functionality in TSPCs. With improper sizing, race conditions may result to output glitches. The width of transistors M_{N2} and M_{N3} should be 2~3 times larger than of the others in order to enhance the charge and discharge ability and avert glitches.

A vernier delay lines is also sensitive to the parasitic capacitances at the inputs of the D flip-flop (Q, CLK in Fig. 3-31). Based on the basic configuration of the vernier delay line, the outputs of the two delay chains are connected to the D-flip-flops directly. There capacitances will affect the delay time of each delay stage. Moreover, these errors will accumulate through entitle delay chains (shown in Fig. 3-31). The capacitances of each input can be estimated to be:

$$\begin{cases} C_{CLK} = C_{MP2} + C_{MP3} + C_{MN3} + C_{MN4} \\ C_{Q} = C_{MP1} + C_{MN1} \end{cases} \tag{3-37}$$

Clearly, the capacitances in these two inputs are not equal. Even if the smallest size of transistors is chosen, the effect of the unequal parasitic capacitance cannot be ignored, when high resolution of the vernier delay line is required. Adding buffers before the D flip-flops can alleviate this issue. An additional benefit of introducing these buffers is they reshape signals after each delay stage, and avoid metastabilty.

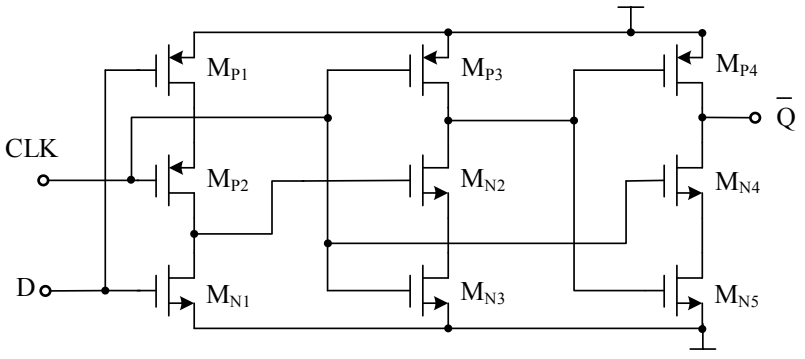


Figure 0-31: Schematic of the TSPC D flip-flop

The residual from linear performance of the proposed delay line is shown in Fig. 3-32. The resolution error of the vernier delay line better than 0.1% in the range from 8.5ns to 51ns.

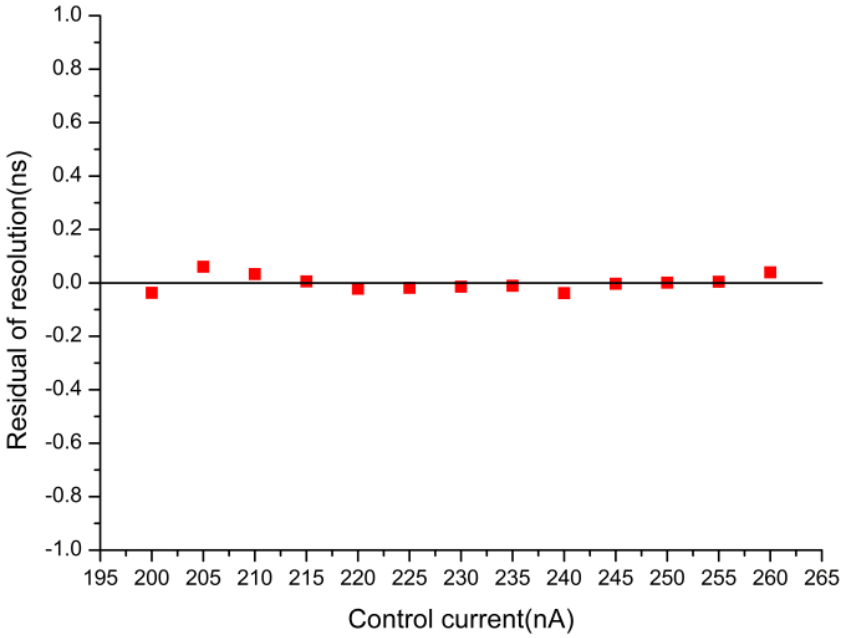


Figure 0-32: Resolution error of the proposed vernier delay line

1.12.2.2 Coarse counter

The configuration of the coarse counter is quite straightforward; it can be realised simply by implementing a count-up or count-down counter. In the proposed implementation, the count-down ripple counter is used as the coarse counter. The ripple counter comprises several divide-by-2 circuits, which can be easily realized by D flip-flops. The configuration is shown in Fig. 3-33. The number of dividers depends on the bits of the counter used in the system. In the proposed implementation, as analysed in the previous section, the 4-bit coarse counter is chosen.

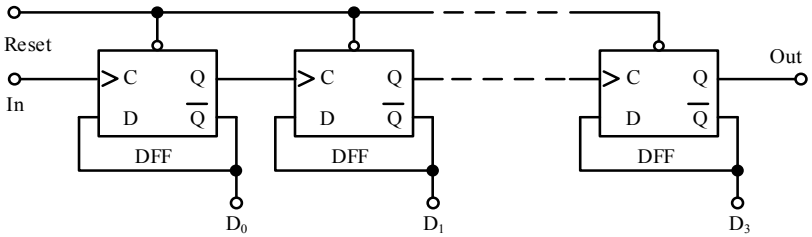


Figure 0-33: Configuration of the coarse counter

1.12.2.3 Thermometer-to-binary code decoder

There are two methods to implement the thermometer to binary code decoder [85]; in terms of the area, the multiplexer-based thermometer-to binary code decoder is the better choice. As an example, 4-bit decoder is shown in Fig. 3-34. In practice, there is a 7-bit thermometer to binary decoder from b0 to b6.

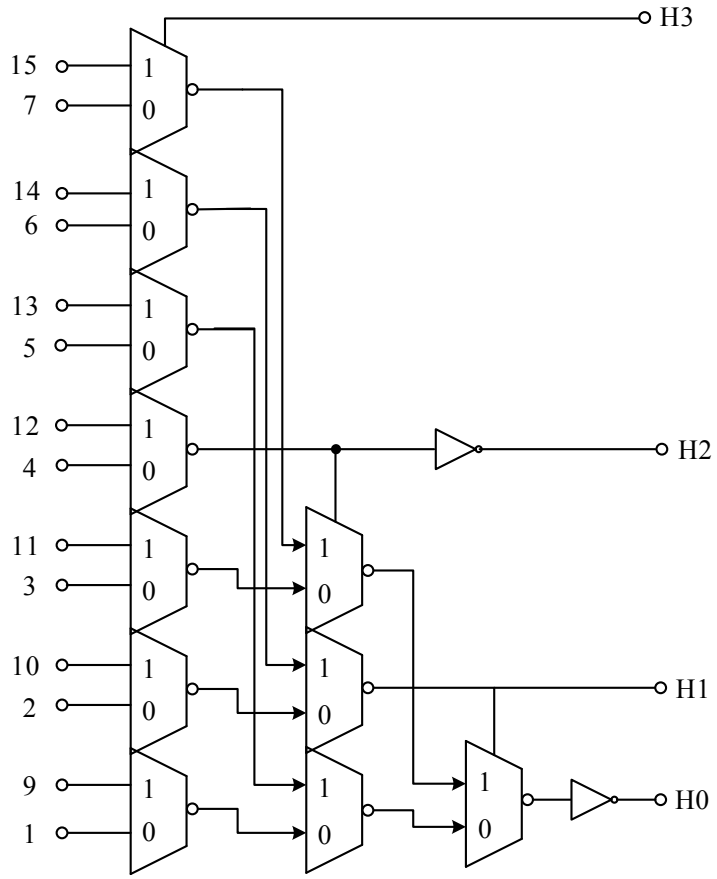


Figure 0-34: Configuration of the thermometer to Binary code decoder (16-to-4 as example)

1.13 Summary

This chapter presents a first order asynchronous sigma delta modulator with time quantisation. The proposed modulator is designed in the AMS $0.35\mu m$ process. The modulator is designed for low frequency applications. The limit cycle of the proposed ASDM is 200kHz and the bandwidth of 3kHz. A special low distortion OTA is used as a loop filter. The input dynamic range of the modulator is from $-100mV$ to $+100mV$. A spurious-free dynamic range of 71.3dB is obtained when the input signal bandwidth is equal to $B/3 = 1kHz$.

A new time quantiser for asynchronous sigma delta modulators is also presented**.** The circuit implements a special coarse-fine time-to-digital converter to quantise the timing of the square wave produced by asynchronous sigma delta modulators. This circuit converts the duty cycle to a digital output. The proposed circuit measures the pulse width and the period separately by implementing a special time-to-digital converter, which utilizes vernier delay lines. This structure can achieve high resolution despite using a low sampling frequency.

The Asynchronous Sigma Delta Modulator with Noise Shaping

1.14 Introduction

The main issue of asynchronous sigma delta modulators is the absence of spectral shaping of the quantisation noise from the time-to-digital converter. A high resolution time-to-digital converter is requirement when ASDMs are implemented in the high accurate application. In order to solve this issue, noise shaping can be introduced to ASDMs. In this chapter, the conventional solution are discussed. And a novel solution is presented here, which overcomes these issues. This chapter includes the system analysis and design of this novel modulator, and the system level simulation are carried out in the Simulink environment of Matlab. The circuit of this modulator is designed in AMS $0.35\mu m$ CMOS technology, and the transistor level simulations are performed on the Spectre simulator of the Cadence Design Framework.

1.15 Conventional asynchronous sigma delta modulator with noise shaping

Conventionally, asynchronous sigma delta modulators can be extended to the configuration shown in Fig. 4.1 [54], to obtain the noise shaping. The digital output of the time-to-digital converter is converted to an analogue signal by a multi-bit digital-to-analogue converter, and fed back to the input. The filter $H_1(s)$ works as an L^{th} order noise shaping filter.

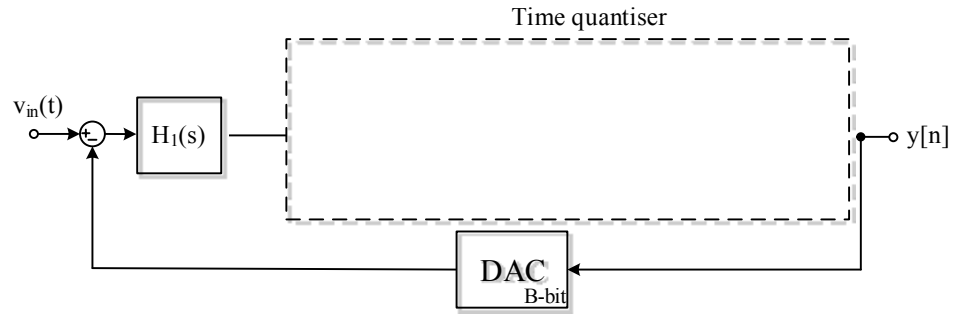


Figure 0-1: System diagram of asynchronous sigma delta modulators with noise shaping

In fact, the system shown in Fig. 4-1 can be seen as a synchronous continuous-time sigma delta modulator, where the normal amplitude quantiser is replaced by a time quantiser including an asynchronous sigma delta modulator and a time-to-digital converter. The corresponding linear model of the system in Fig.4-1 is shown in Fig. 4-2.

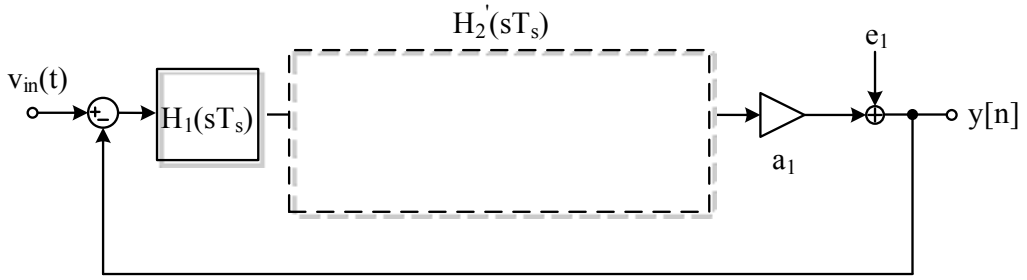


Figure 0-2: Corresponding model with NRZ DAC

The transfer function can be described as:

$$y = STF\left(sT_s\right)X\left(s\right) + NTF_1\left(sT_s\right)e_1 \tag{4-1}$$

Where $X\left(s\right)$ is the s-domain of the input signal; e_1 is the quantisation errors in TDC; whereas $SFT\left(sT_s\right)$ and $NTF\left(sT_s\right)$ are the respective transfer functions, given by:

$$\begin{cases} SFT\left(sT_s\right) = \dfrac{H_1\left(sT_s\right)\cdot H_2'\left(sT_s\right)}{1+H_1\left(sT_s\right)\cdot H_2'\left(sT_s\right)} \\ NTF_1\left(sT_s\right) = \dfrac{H_2'\left(sT_s\right)}{1+H_1\left(sT_s\right)\cdot H_2'\left(sT_s\right)} \\ NTF_2\left(sT_s\right) = \dfrac{1}{1+H_1\left(sT_s\right)\cdot H_2'\left(sT_s\right)} \end{cases} \tag{4-2}$$

Where $H_2'\left(sT_s\right) = \dfrac{H_2\left(sT_s\right)}{1+H_2\left(sT_s\right)\cdot T}$.

The advantage of the configuration in Fig. 4-1 is that it provides noise shaping not only for the quantisation error in time-to-digital converter, but also for the distortion error in ASDM. This is because the distortion error in ASDM can be considered as an error e_1 added into the system as shown in Fig. 4-2, which is shaped by the loop filter $H_1(s)$. For a first order loop filter $H_1(s)$, the configuration performs L^{th} order noise shaping. The SNR of the system can be derived as:

$$SNR = \frac{6\pi^{2L}V^2}{2L+1}\left(1-V^2\right)^{2L-1} \cdot F^{2L-1} \cdot OSR^2 \tag{4-3}$$

Where V is the normalized input amplitude; $OSR = f_s/2B$; $F = f_c/2B$.

Fig. 4-3 illustrates the difference between ASDMs with and without noise shaping. For the noise shaping system (upper black line), the SNR of the system is increased by 14dB with the same sampling clock, when the input signal is less than -10dB. When the input signal is larger than -10dB, the phase modulation phenomenon significantly increases, which reduces the performance of the noise shaping. While for the conventional open loop system (the lower red line), the OSR is significantly increased when the input amplitude is over -10dB. And when the maximum signal is applied ($V = 0.8$), the two systems have the same SNR.

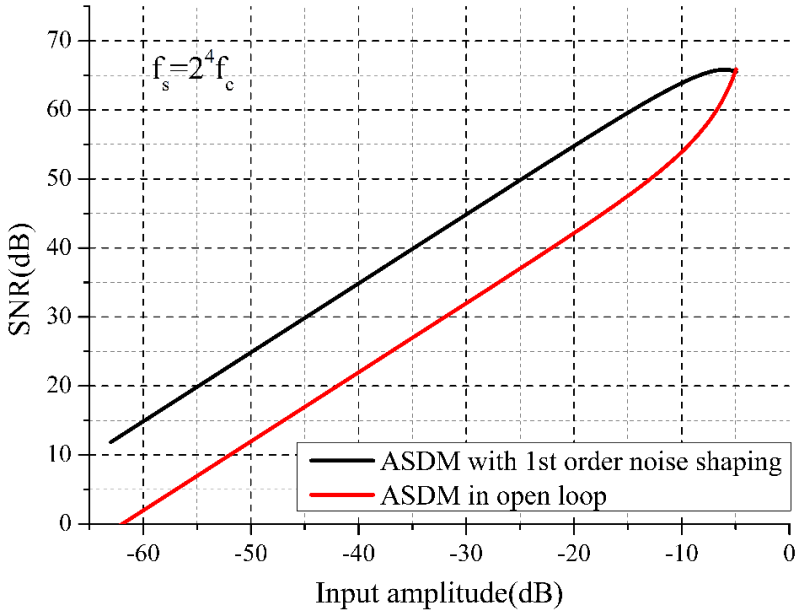


Figure 0-3: SNR comparison between ASDMs with/without noise shaping

When considering the distortion of ASDMs, the comparison of SNDR of two systems is shown in Fig. 4-4. The result is quite similar. When the normalized input amplitude is over 0.7, the open loop system has better performance of the system with first order noise shaping. This conclusion is reversed when the normalized input amplitude is smaller than 0.7.

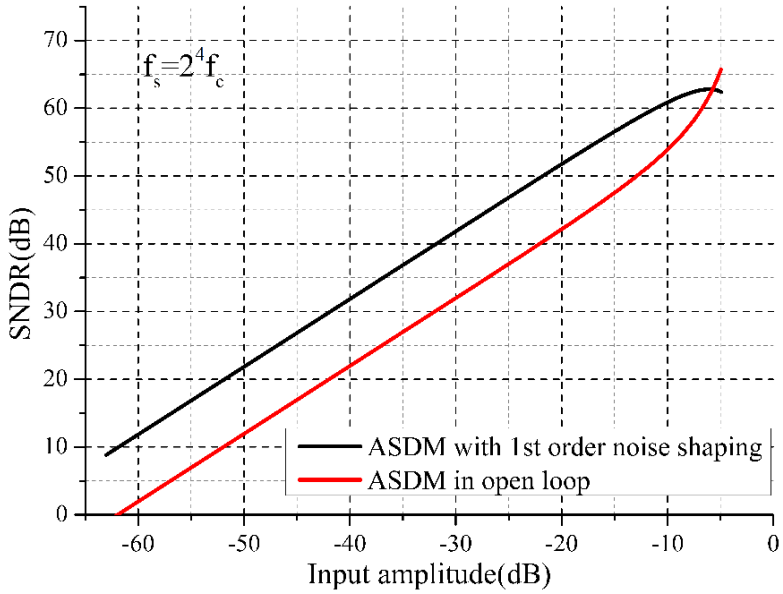


Figure 0-4: SNDR comparison between ASDMs with and without noise shaping ($f_{in} = B/3$)

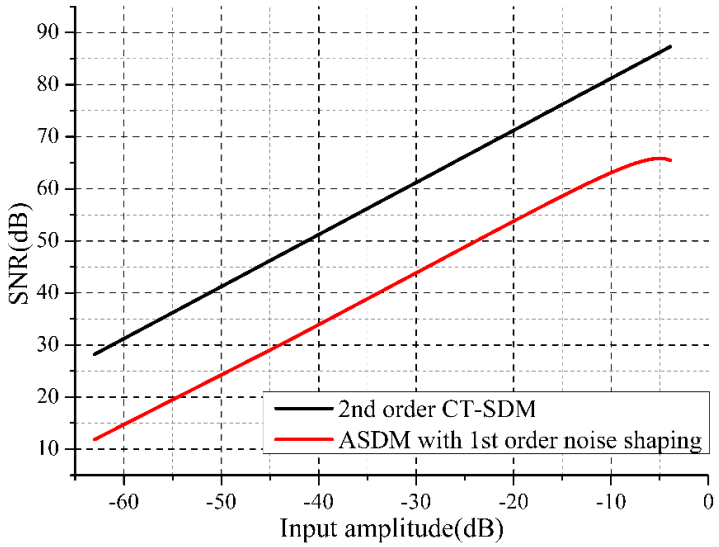


Figure 0-5: SNR comparison between the ASDM with 1st order noise shaping and the 2nd order continuous-time-SDM

The main issue of the ASDM with noise shaping in Fig. 4-1 is that an L^{th} order system only brings $(L-1)^{th}$ noise shaping. Figure: 4-5 shows the comparison of SNR between the ASDM and continuous-time SDM, both of them are 2nd order system. It is clear that, with the same sampling clock, the synchronous continuous-time SDM has much better performance than the ASDM with noise shaping. So we can simply conclude that the configuration in Fig. 4-1 will increase the performance of the system when the normalized input signal is smaller than 0.7. However, when compared with the conventional synchronous SDM with same order and with the sampling clock, this configuration has poor performance. Therefore, this configuration is not a good implementation for ASDMs with noise shaping. More details are listed in Table 4-1.

Table 0-1: Comparison between ASDM with/without noise shaping and synchronous CT-SDM

	ASDM with open loop	ASDM with 1st order noise shaping	2nd order synchronous CT-SDM
System order	1	2	2
Noise shaping	Null	1st order	2nd order
Clock jitter	Immune	Sensitive	Sensitive
Excess loop delay	Distortion	Distortion + Instability	Instability
Quantiser	TDC	ASDM + TDC	Sampled comparator
DAC	Null	Multi-bit	Signal/Multi-bit

1.16 A novel asynchronous sigma delta modulator with noise shaping

For a conventional sampling solution, multiple phase sampler can be implemented to reduce the requirement of the sampling frequency [46]. Here I introduce a novel asynchronous sigma delta modulator as shown in Fig.4-6, where the poly-phase sampler is moved into system loop as a multi-bit quantiser. And a special digital-to-time converter is used in feedback loop to reconstruct the feedback signal. This novel system introduces a first order noise shaping without adding any other loop filter, and require only a single-bit DTC in the feedback even for the multi-bit quantiser.

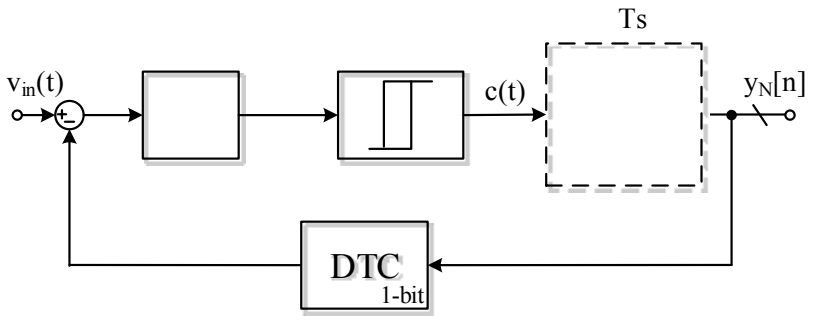


Figure 0-6: Configuration of the proposed asynchronous sigma delta modulator

1.16.1 System analysis

Compared with Fig. 4-1, only one feedback loop is in the proposed configuration. The multi-bit feedback back digital-to-analogue converter is replaced by a simple single-bit digital-to-time converter, which increases the free degree of design. The configuration in Fig. 4-6 is similar with that of synchronous continuous-time sigma delta modulators. Fig. 4-7 shows the signal flow of the proposed ASDM and the conventional CT-SDM, respectively. The main difference between these two configurations is in the proposed ASDM (Fig. 4-7 (a)), the sample is taken after the comparator, which is continuous time. This is contrast to conventional CT-SDMs (Fig. 4-7 (b)) where the sample is taken after the loop filter, and then the signal is fed into a timed comparator or quantiser. The proposed system is still asynchronous, because the decision of the comparator (quantiser) is not controlled by the sample clock, but is trigged by the input signal. Another difference is the feedback loop. In the proposed one, a single-bit DTC is implemented as a counter counting cycles of the sample clock in one measuring event with a N channels output. In the CT-SDMs, an equivalent N channels DAC is required.

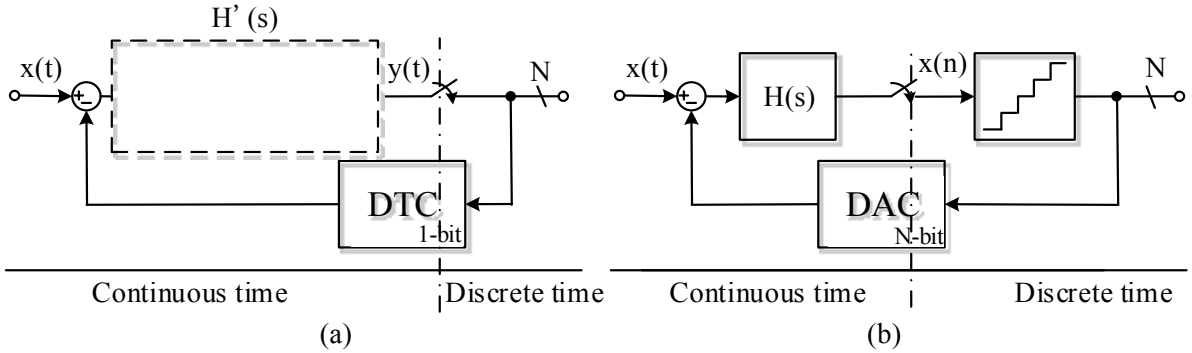


Figure 0-7: Comparison of (a) the proposed ASDM and (b) the conventional CT-SDM

Fig. 4-8 shown the feedback loop of the proposed ASDM. As with discrete-time (DT) to continuous-time (CT) conversion implemented in CT-SDMs, the noise transfer function can be given by:

$$NTF = \frac{1}{1 + H'(s)F(v)} \tag{4-4}$$

Where $H'(s) = R(s)H(s)$ is the equivalent transfer function; $R(s)$ is the s-domain of the DTC; $F(v)$ is the transfer function of voltage-to-time converter.

On each channel of the DTC there is a non-return zero (NRZ) waveform. Similarly to the argument in Chapter 2, the system analysis for the proposed ASDM can be divided as two sections: (a) a constant input signal and (b) dynamic input signal.

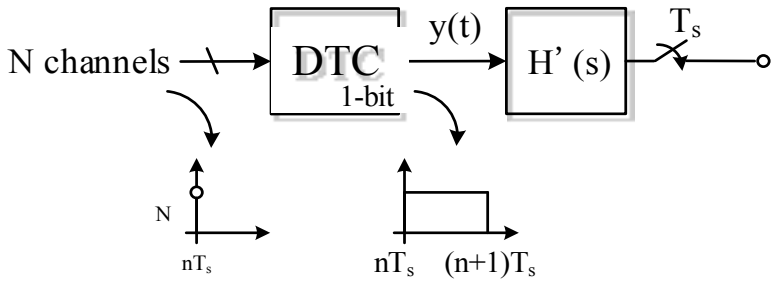


Figure 0-8: Feedback loop of the proposed ASDM

1.16.1.1 A constant input signal $v_{in} = V$ $(|V| < 1)$

Here the equation of the square wave with duty cycle can be rewritten as:

$$y(t) = 2\alpha - 1 + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin n\alpha\pi}{n}\cos n\omega t \tag{4-5}$$

Where $\alpha = (1+V)/2$ is the duty cycle.

The data signal after sampling can be described as:

$$y(n)=\sum_{k=0}^{N} y(t)\delta(t-k\tau_0) \tag{4-6}$$

Where $\tau_0 = T_s/M$ is the resolution of the delay chain; M is the length of the delay chain.

The digital-to-time converter here works as the simplicity digital-to-analogue converter, which is assumed to have a zero-order-hold (ZOH) transfer function. For the NRZ waveform, the reconstructed feedback signal can be obtained as:

$$y'(t)=\sum_{k=0}^{N} y(t)\delta(t-k\tau_0)\otimes R(t) \tag{4-7}$$

Where $R(t)=u(t)-u(t-\tau_0)$.

By inserting eq. (4-6), the feedback signal is:

$$y'(t)=\sum_{k=0}^{N}\left[(2\alpha-1)+\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin n\alpha\pi}{n}\cos n\omega k\tau_0\right]R(t-k\tau_0) \tag{4-8}$$

According to eq. (2-13), the output of the loop filter can be written as:

$$\begin{aligned} c(t)=&\left[V-(2\alpha-1)\right]\mathrm{Re}\,H(0)\\ &-\frac{4}{\pi}\sum_{k=0}^{N}\sum_{n=1}^{\infty}\frac{\sin n\alpha\pi}{n}\left[\mathrm{Re}\,H(n\omega)\cos n\omega k\tau_0-\mathrm{Im}\,H(n\omega)\sin n\omega k\tau_0\right] \end{aligned} \tag{4-9}$$

Where $H(\omega)$ is Fourier form of the loop filter.

Slightly different with eq. (2-15), the boundary conditions here can be shown to be:

$$\begin{cases} t_1 = mT_0-\dfrac{1}{2}T_1 = k_1\tau_0+\varepsilon, & c(t_1)=-b \\ t_2 = mT_0+\dfrac{1}{2}T_1 = k_2\tau_0+\varepsilon, & c(t_2)=b \end{cases} \tag{4-10}$$

Where $|\varepsilon| \in [0, \tau_0]$ is the quantisation error.

Inserting the boundary conditions will result in:

$$\begin{cases} V-(2\alpha-1)=\dfrac{2}{\pi}\displaystyle\sum_{n=1}^{\infty}\dfrac{\sin 2\alpha n\pi}{n\,\mathrm{Re}\,H(0)}\left[\mathrm{Re}\,H(n\omega_0)\cos 2n\pi\dfrac{\varepsilon}{T_0}+\mathrm{Im}\,H(n\omega_0)\sin 2n\pi\dfrac{\varepsilon}{T_0}\right] \\ \displaystyle\sum_{n=1}^{\infty}\dfrac{\sin^2\alpha n\pi}{n}\left[\mathrm{Re}\,H(n\omega_0)\sin 2n\pi\dfrac{\varepsilon}{T_0}+\mathrm{Im}\,H(n\omega_0)\cos 2n\pi\dfrac{\varepsilon}{T_0}\right]=\dfrac{b\pi}{4} \end{cases} \quad (4\text{-}11)$$

Where

$$\cos n\omega_0 k_1\tau_0=\cos n\omega_0(t_1-\varepsilon)=\cos\left(\alpha n\pi-2n\pi\frac{\varepsilon}{T_0}\right)$$

$$\cos n\omega_0 k_2\tau_0=\cos n\omega_0(t_2-\varepsilon)=\cos\left(\alpha n\pi-2n\pi\frac{\varepsilon}{T_0}\right)$$

$$\sin n\omega_0 k_1\tau_0=\sin n\omega_0(t_1-\varepsilon)=-\sin\left(\alpha n\pi-2n\pi\frac{\varepsilon}{T_0}\right)$$

$$\sin n\omega_0 k_2\tau_0=\sin n\omega_0(t_2-\varepsilon)=\sin\left(\alpha n\pi+2n\pi\frac{\varepsilon}{T_0}\right)$$

and T_0 is the output frequency of the ASDM.

Clearly, when $\tau_0 \to 0$, the quantisation error ε becomes zero, the equation above becomes that of the conventional ASDM given in Chapter 2. Inserting $\alpha=(V+1)/2$ into eq. (4-11) gives:

$$V-(2\alpha-1)=\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{(-1)^n\sin n\pi V}{n\,\mathrm{Re}\,H(0)}\left[\mathrm{Re}\,H(n\omega_0)\cos 2n\pi\frac{\varepsilon}{T_0}+\mathrm{Im}\,H(n\omega_0)\sin 2n\pi\frac{\varepsilon}{T_0}\right] \quad (4\text{-}12)$$

For a loop filter with non-zero single pole is:

$$H(\omega)=\frac{a}{j\omega+p} \tag{4-13}$$

Inserting eq. (4-13) to eq. (4-12) will results in:

$$2\alpha-1=V\left(1+\beta-\beta\frac{\pi^2}{3}V^2\right) \tag{4-14}$$

Where $\beta=\sqrt{2}\frac{p}{\omega_0}\sin\left(2\pi\frac{\varepsilon}{T_0}+\frac{\pi}{4}\right)$.

Assuming that $p/\omega_0 << 1$, the duty cycle is quasi proportional to the normalized amplitude of the input signal, which is the same as the conclusion obtained in Chapter 2. For an ideal integrator $H(\omega)=\frac{1}{j\omega}$ ($p=0$), β becomes zero, and the right hand of eq. (4-14) becomes V.

Therefore, for a constant input V ($|V|<1$) signal, the duty cycle of the proposed ASDM is proportional to the input, as it the case with the conventional ASDM.

1.16.1.2 Dynamic input signal $v_{in}=V\cos\mu t$ ($|V|<1$)

Similar to Chapter 2, the same assumption is applied: the variation of the input signal is much slower than the limit cycle frequency. Hence the equation of the input signal can be rewritten as:

$$v_{in}=V\cos\mu t\approx V\sum_{m=0}^{M}\cos\mu T_m=V\sum_{m=0}^{M}\sum_{k=0}^{N}\cos\mu\left(k\tau_0\right)_m \tag{4-15}$$

During the period of $T_m\le t\le T_{m+1}$, the output of the loop filter $c(t)$ can be given by:

$$\begin{aligned}c(t)_m=&\left[V\cos\mu T_m-(2\alpha-1)\right]\sum_{k=0}^{N}\left[\mathrm{Re}\,H(\mu)\cos\mu k\tau_0-\mathrm{Im}\,H(\mu)\sin\mu k\tau_0\right]\\&-\frac{4}{\pi}\sum_{k=0}^{N}\sum_{n=1}^{\infty}\frac{\sin n\alpha\pi}{n}\left[\mathrm{Re}\,H(n\omega)\cos n\omega k\tau_0-\mathrm{Im}\,H(n\omega)\sin n\omega k\tau_0\right]\end{aligned} \tag{4-16}$$

By inserting the boundary conditions (eq. (4-10)), the following equations can be obtained:

$$\begin{cases} V\cos\mu T_m-\left(2\alpha_m-1\right)=\dfrac{2}{\pi}\displaystyle\sum_{n=1}^{\infty}\dfrac{\sin 2\alpha_m n\pi}{n\,\mathrm{Re}\,H\left(\mu\right)\cos\mu T_m} \\ \qquad\qquad\qquad\qquad\times\left[\mathrm{Re}\,H\left(n\omega_m\right)\cos 2n\pi\dfrac{\varepsilon}{T_m}+\mathrm{Im}\,H\left(n\omega_m\right)\sin 2n\pi\dfrac{\varepsilon}{T_m}\right] \\ \dfrac{4}{\pi}\displaystyle\sum_{n=1}^{\infty}\dfrac{\sin^2\alpha_m n\pi}{n}\left[\mathrm{Re}\,H\left(n\omega_m\right)\sin 2n\pi\dfrac{\varepsilon}{T_m}+\mathrm{Im}\,H\left(n\omega_m\right)\cos 2n\pi\dfrac{\varepsilon}{T_m}\right]=b \end{cases} \tag{4-17}$$

Where $k_1\tau_0,k_2\tau_0\in\left[T_m,T_{m+1}\right]$; $\cos\mu k_1\tau_0\approx\cos\mu k_2\tau_0\approx\cos\mu T_m$; $\sin\mu k_1\tau_0\approx\sin\mu k_2\tau_0\approx\sin\mu T_m$ ($\mu<<\omega_m$).

Again, insertion of $\alpha_m=\left(V\cos\mu T_m+1\right)/2$, results in:

$$\begin{aligned} V\cos\mu T_m-\left(2\alpha_m-1\right)&=\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\left(-1\right)^n\sin\left(n\pi V\cos\mu T_m\right)}{n\,\mathrm{Re}\,H\left(\mu\right)} \\ &\quad\times\left[\mathrm{Re}\,H\left(n\omega_m\right)\cos 2n\pi\frac{\varepsilon}{T_m}+\mathrm{Im}\,H\left(n\omega_m\right)\sin 2n\pi\frac{\varepsilon}{T_m}\right] \end{aligned} \tag{4-18}$$

For an ideal integrator filter, eq. (4-18) can be rewritten as:

$$2\alpha_m-1=V\cos\mu T_m+\frac{A}{24}V\cos\mu T_m-\frac{\pi^2}{24}AV^3\cos 3\mu T_m \tag{4-19}$$

Where $A=\sqrt{2}\left(\dfrac{1}{F_m}\right)^2\sin\left(2\pi\dfrac{\varepsilon}{T_m}+\dfrac{\pi}{4}\right)$; $F_m=\dfrac{\omega_m}{\mu}$.

It is interesting to notice that, for the proposed ASDM, the most significant distortion is still the third order harmonic distortion, shown in eq. (4-20). Similar to the effect of the propagation delay

analysed in Chapter 2, the quantisation errors will slightly increase the distortion, and will lead maximum 3dB lose in SFDR.

$$\Delta_3 \approx \frac{\pi^2\sqrt{2}}{24}\left(\frac{1}{F_m}\right)^2 V^3 \sin\left(2\pi\frac{\varepsilon}{T_m}+\frac{\pi}{4}\right) \tag{4-20}$$

The mean value of output can be written as:

$$\bar{y}[n]=\frac{T_p[n]-T_n[n]}{T_c}=\frac{(n_1-n_2)\tau_0+mT_s}{T_c} \tag{4-21}$$

Where n_1 and n_2 are the adjacent output thermometer code of the sampler; $T_p[n]$ and $T_n[n]$ are the reconstruction waveforms.

When the amplitude of the input signal is less than -10dB, according to eq. (2-3), the maximum variation of T_c is less than 10%. Therefore, the T_c can be considered as constant. Hence, the minimum quantisation step is:

$$\Delta=\bar{y}[n+1]-\bar{y}[n]=\frac{\tau_0}{T_0}=\frac{1}{N}\cdot\frac{f_0}{f_s} \tag{4-22}$$

Obviously, the higher resolution of the delay chain, the greater the degree of mismatch between the asynchronous limit cycle output and the waveform after reconstruction, and the mismatch errors ε is reshaped by a first-order noise shaping. The in-band power of the quantisation error can be written as:

$$P_q=\frac{\Delta^2}{12f_c}\int_{-B}^{B} NTF^2 df \propto \frac{B^2}{F\cdot(N\cdot f_s)^2\cdot(1-V^2)} \tag{4-23}$$

Therefore, the SQNR (signal-to-quantisation noise ratio) of the system will be

$$SQNR \propto V^2 \cdot \left(\frac{N \cdot f_s}{B}\right)^2 \cdot F \cdot \left(1 - V^2\right) \tag{4-24}$$

Where $F = f_c / 2B$; B is the signal bandwidth; N is length of the delay chain.

Therefore, the SNDR of the system can be derived as:

$$SNDR \propto \frac{V^2}{Sum\left\{p_q, \Delta_3^{\,2}\right\}} \tag{4-25}$$

Fig. 4-9 shows the estimation of SNDR for both ASDM with/without noise shaping. Note that with benefits of the noise shaping, the SNDR is significantly improved when the input signal is smaller than -10dB, where the quantisation errors are dominant. The improvement is approximate 25dB. While when the input signal is larger then -10dB, the SNDR is slightly dropped off. This is because the distortion is increased significantly.

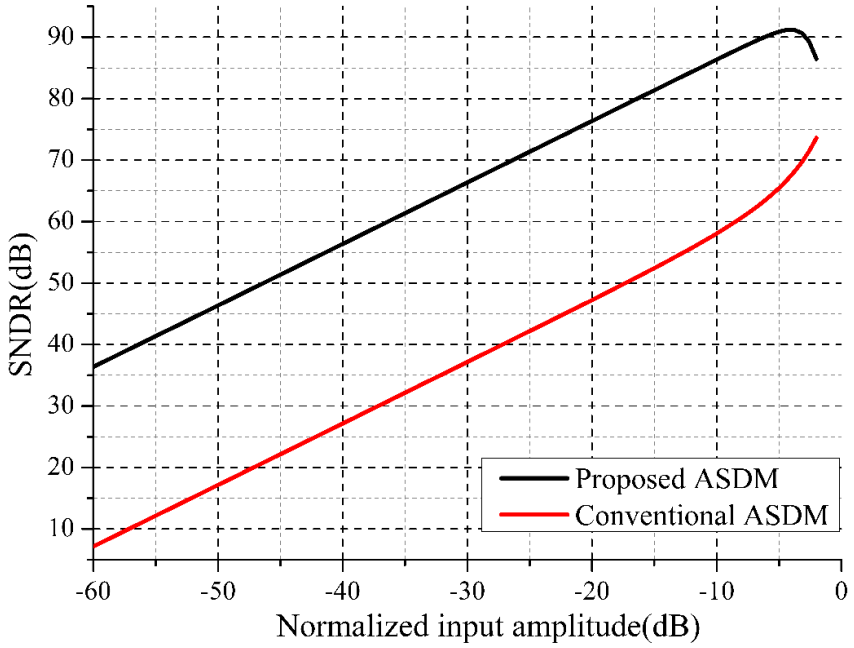


Figure 0-9: Estimation of achieved SNDR of conventional and proposed ASDM

1.16.2 System level design

The configuration of proposed the sampler is shown in Fig. 4-10. The poly-phase sampler consists a delay line and hold block. The sample clock is divided by an N length delay chain to generate multi-phase sample signals, which samples the date signal and generates N channel discrete outputs. The hold block in each channel includes two D flip-flops triggered by each sample phase, in order to avoid metastability [86]. The timing diagram of the sampling process and signal reconstruction is shown in Fig. 4-11. In each sampling period, the poly-phase phase sampler generates N channels thermometer codes (output0~3 in Fig. 4.11). The time interval can be described as:

$$T_{in}[n] = nT_s + (N_r - N_f)\tau_0 \tag{4-26}$$

Where n is the cycle of sample clock; N_r and N_f are the location of the rising and falling edges of the data signal in one period of the sample clock.

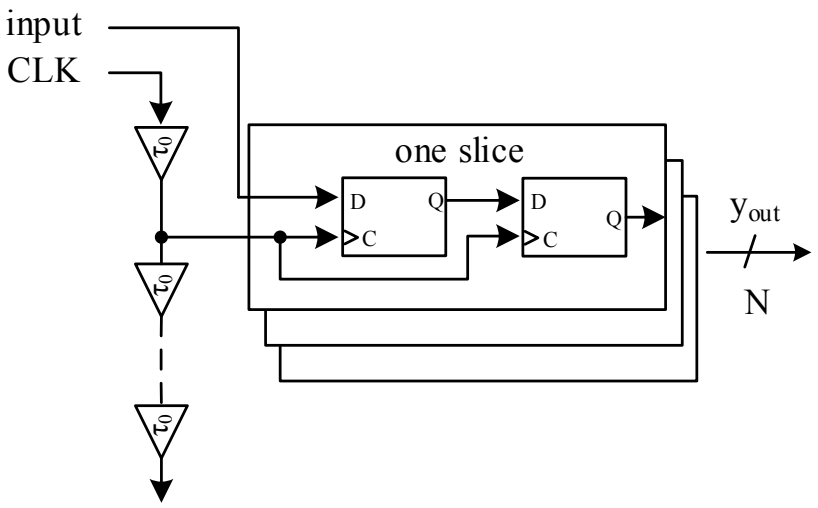


Figure 0-10: Configuration of the proposed multi-poly phase sampler

The outputs of sampler are fed into a digital-to-time converter to generate an equivalent feedback signal. The digital-to-time converter works as a period counter, which consists of OR, NAND logical and a phase detector, as shown in Fig. 4-12. The phase detector is realized by an edge triggered D latch, which detects the rising edge of the output of the NAND gate and generates a

reset signal. By feeding them to an AND gate, a discrete-level square wave feedback signal is generated (feedback in Fig, 4.13).

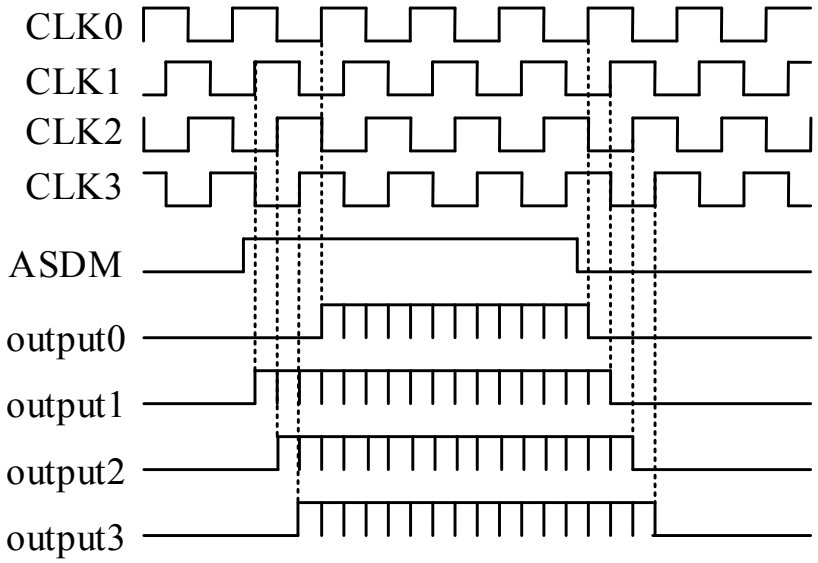


Figure 0-11: Timing diagram for the poly-phase sampling ($N = 4$)

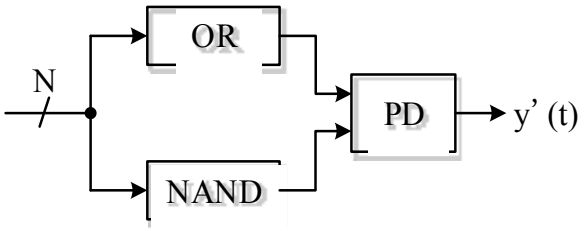


Figure 0-12: Configuration of the time-to-digital converter

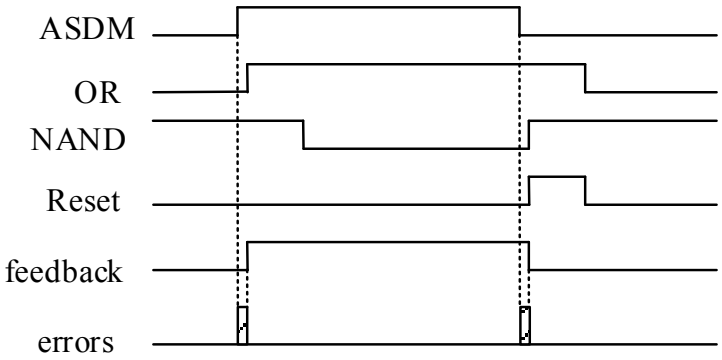


Figure 0-13: Timing diagram for the time-to-digital converter

The error between original time interval and the reconstruction signal (shown in Fig. 4-13) can be described as:

$$e = T - T_{fb}[n] \tag{4-27}$$

This error includes two components: the main part is the quantisation error caused by the sampling process; the other one is transfer delay time caused by the logic gates.

Fig. 4-14 shows the PSD simulation results of ASDMs with and without noise shaping obtained under the Matlab Simulink. An active RC integrator with finite open loop gain is implemented here, and the output signals are filtered by a second order Butterworth low-pass filter. Fig. 4-14 (a) shows the PSD of the conventional ASDM. Notice that the SNDR is limited by the quantisation noise. While, for the proposed ASDM (Fig. 4-14 (b)), the noise performance is limited by the third order harmonic distortion as analysed in the previous section. With the same sampler, because of the benefits of the noise shaping, the SNDR of the proposed ASDM is approximately 19dB better than that of the conventional ASDM.

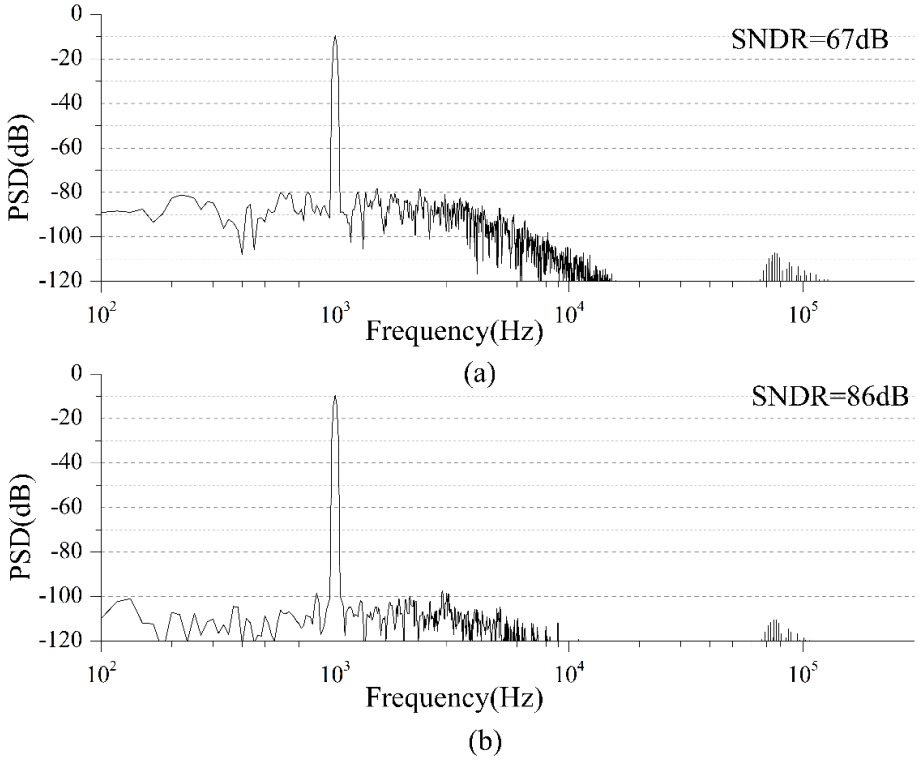


Figure 0-14: PSD of ASDMs with 8 phases sampler with sampling clock of 2MHz, and following a 2nd order LP filter (a) Conventional ASDM; (b) Proposed ASDM

1.16.3 Non-ideal effects in proposed ASDM

In this section, I will describe some implementation problems and practical imperfections of circuits of this novel architecture.

1.16.3.1 Propagation loop delay

In Chapter 2, we have demonstrated the main problem of asynchronous sigma delta modulator is the propagation loop delay, which will increase the distortion of ASDMs. In the proposed architecture, the loop delay includes two parts: one is the delay in the continuous time loop filter and comparator the same as that in the conventional ASDM; the other one is the logic gate transfer delay in the sample & hold block and the feedback signal generator.

For the delay in the analogue parts, as explained in chapter 2, the propagation delay will contributed a factor of $\sqrt{2}\sin\left(2\pi\frac{\Delta\tau}{T_c}+\frac{\pi}{4}\right)$ to the significant harmonic distortion of the system, when a sine input wave is applied. This is similar in magnitude to the contributions to the distortion of quantisation errors (eq. (4-20)). Therefore, we can normalize this propagation delay as the additional part of the quantisation error, the same method can be implemented to the logic gate delay in the sample & hold block and the digital-to-time converter. However, compared with the propagation delay in the analogue parts, the delay in the logic gate is so small that it can be ignored.

1.16.3.2 Clock jitter performance

In the proposed architecture, the system will also suffer the effect of the clock jitter. The main reason of this is different with that in a conventional CT-SDM, where jitter causes unequal pulse areas in the feedback DAC. The jitter effect in the proposed architecture is mainly caused by the jitter in the sampling clock. As mentioned before, the feedback of the proposed ASDM is a digital-to-time converter, which counts the cycles of the sampling clock in each measurement. Hence the unequal pulse areas caused in the sampling clock will contribute the pulse variation in the reconstruction feedback signal, where the clock jitter will accumulate in the digital-to-time converter. This noise induced by the clock jitter is spectrally shaped by the loop provided that its power is finite. This power is proportional to the derivation of the input signal and the open loop gain of the modulator. Hence in a practical implementation it is always a shaped component,

although its variance may be high enough to be a significant source of bit loss. According to the analysis in [6], the in-band noise power due to the jitter in proposed DTC can be derived as:

$$P_\sigma = \frac{N\sigma^2}{f_0}\int_{-B}^{B} H^2 df \tag{4-28}$$

Where N is the number of the cycle of the sampling clock in one time interval.

To compute this effect, a simulation is taken including jitter in the clock, as shown in Fig. 4-15. The SNR of the proposed modulator will reduce 12dB with the clock jitter of 10%T_s. Meanwhile, the clock jitter will also increase the distortion of ASDMs, as it will contribute the total loop delay in the system.

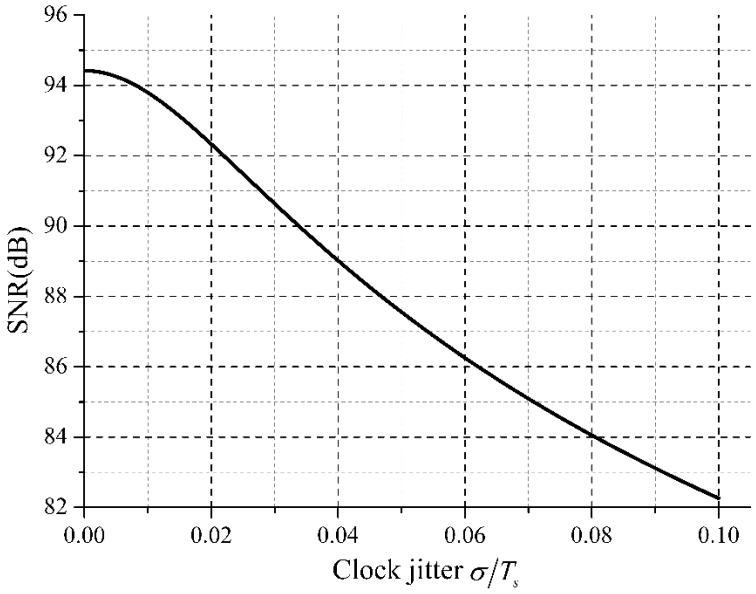


Figure 0-15: Clock jitter performance of the proposed ASDM

4.3.4 Circuit level design

The signal bandwidth of the proposed system is 3kHz, and the limit cycle frequency is set to be 200kHz. The sample clock is 2MHz and divided by an 8-stage delay chain to generate 8 channel digital outputs.

1.16.3.3 Loop filter and comparator

The configurations of the Gm-C integrator and the continuous-time comparator implemented here are the same as that used in Chapter 3. Considering the non-ideal performance of the integrator (pole is not zero, Fig. 2-10), the pole frequency of the loop filter must be smaller than the signal bandwidth. In this implementation, the Gm value of the OTA is set to be $8.3\mu S$, as shown in Fig. 4-16. More details of the integrator and comparator are listed in Table 4-2.

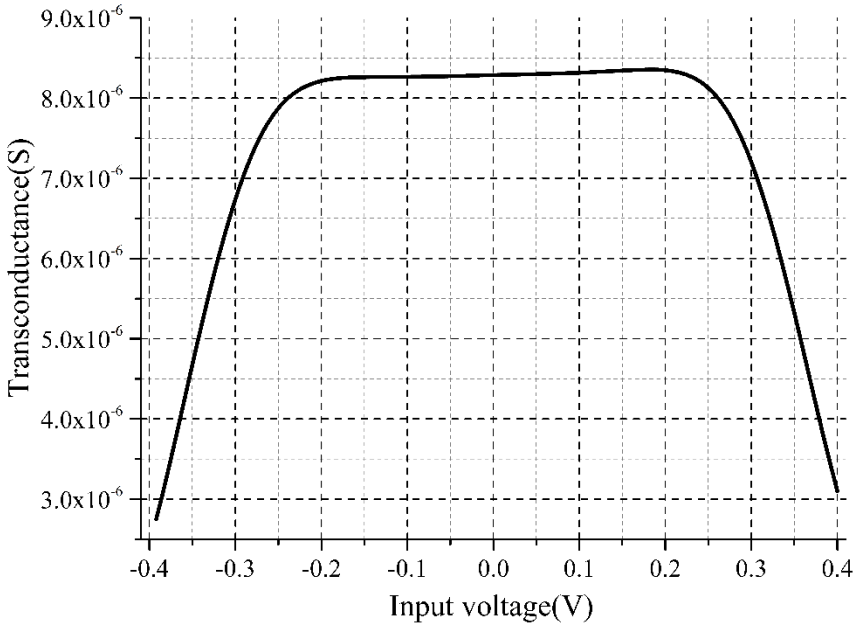


Figure 0-16: Transconductance of the OTA versus input voltage

Table 0-2: Main parameters of the integrator and comparator

	Parameters	Performance
Gm-C integrator	Supply voltage	$\pm 1.5V$
	Bandwidth ($-3dB$)	$4kHz$
	Input dynamic range	$\pm 200mV$
	The 3rd order distortion	$< -60dB$
	Loop pole	$300Hz$
Comparator	Supply voltage	$\pm 1.5V$
	Open loop gain	$43.6dB$
	Bandwidth ($-3dB$)	$400kHz$
	Slew rate	$65V/\mu s$

1.16.3.4 Delay chain

The architecture of the delay chain in the poly-phase sampler is shown in Fig. 4-18. In the implementation, eight delay elements are used in the delay chain. The delay time of each delay element is:

$$\tau = \frac{C}{I_{cp}} V \tag{4-29}$$

Where I_{cp} is the charge/discharge current, which is controlled by the gate voltage of M_{N1} and V is the swing voltage.

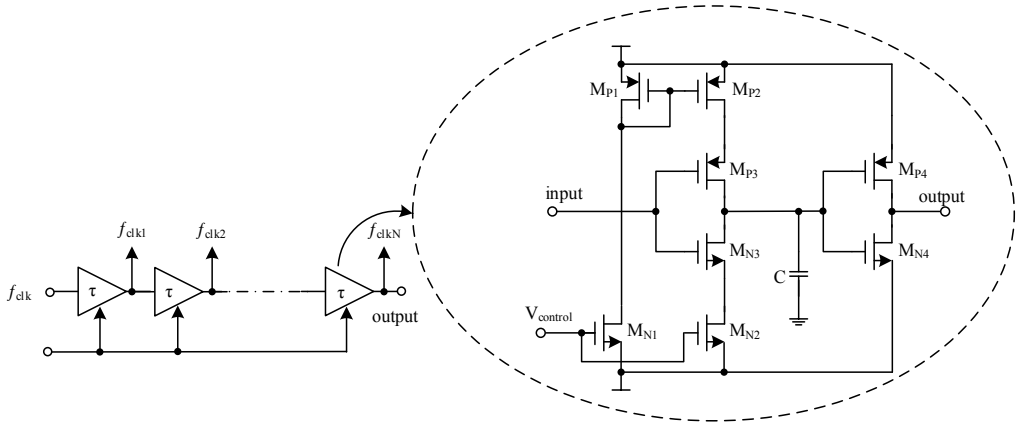


Figure 0-17: Configuration of the delay chain

The delay time of each delay element is set to be 64ns. Table 4-3 lists the transistor sizes of the delay element shown in Fig. 4-17. The main issue of the delay chain is variation caused by the mismatch and process variation. Fig. 4-18 shows Monte Carlo simulation of one delay elements. Note that the variation of the delay time is within the range between 54ns to 78ns. The maxim variation Δt_0 is smaller than $0.2\Delta\tau$ for one delay element. While, the totally maxim variation of the delay chain ($N = 8$) is derived as:

$$\Delta t_{total} = \sqrt{N}\Delta t_0 \le 0.57\Delta\tau \tag{4-30}$$

Table 0-3: Sizes of transistors in one delay element

Transistor	Size (W/L)
M_{P1},M_{P2},M_{P3},M_{P4}	$6\mu m/20\mu m$
M_{N1},M_{N2},M_{N3},M_{N4}	$2\mu m/20\mu m$

Another main issue of the delay chain is the temperature, Fig. 4-19 shows the delay time variation of one delay element versus temperature. The temperature coefficient of one delay element is $3125 ppm/°C$. To minimize the effects, including process variation, mismatch and temperature, a delay-locked loop can be implemented. However, it will increase the complexity of the system, as well as the power consumption.

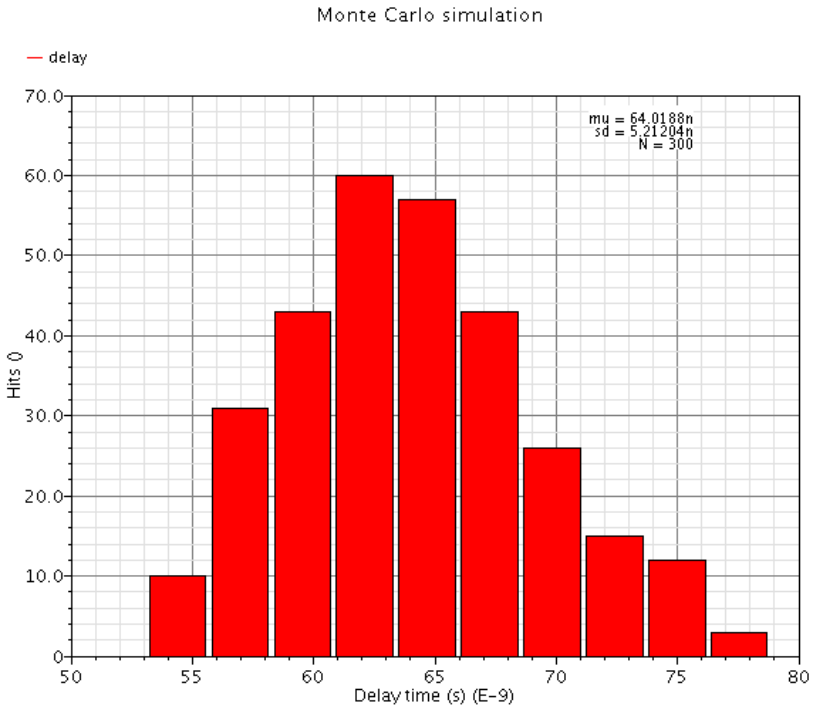


Figure 0-18: Monte Carlo simulation for one delay element

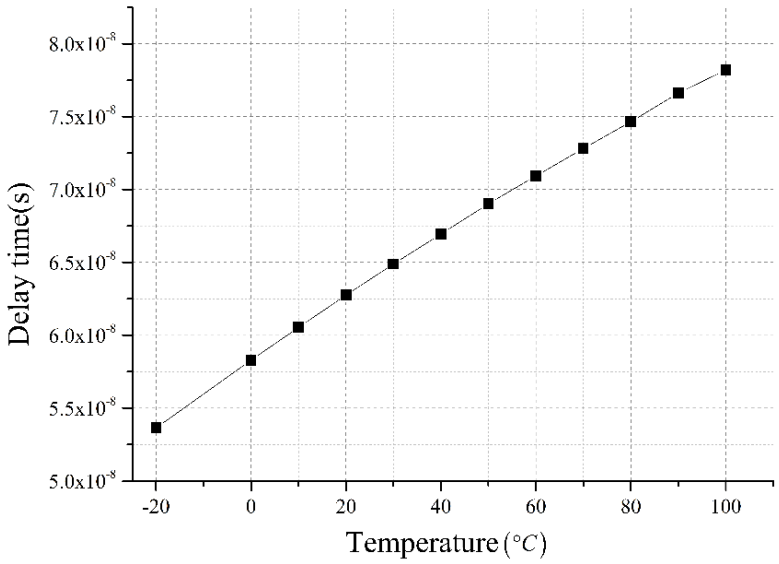
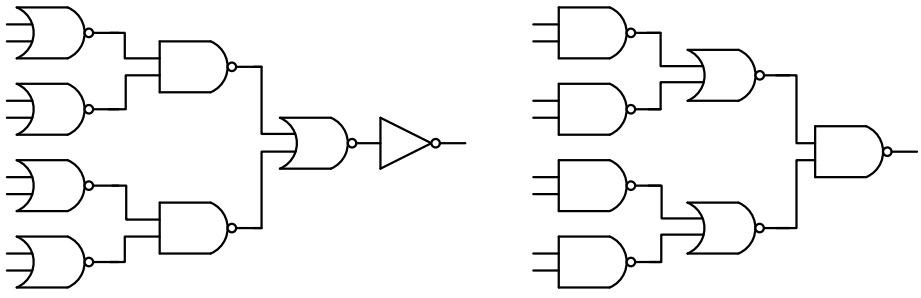


Figure 0-19: Variation of the delay time versus temperature

1.16.3.5 Digital-to-time converter

The digital-to-time converter is designed in the digital domain. All the logic gates are designed with static complementary CMOS style, because of its many advantages including low sensitivity to noise good performance, and low power consumption (with no static power consumption). In order to reduce fan-in requirements (and this way minimizes the propagation delay), the eight-input OR gate and NAND gate are restructured, as shown in Fig. 4-20. All input signals are configured in parallel form to avoid glitches.



(a) 8-input OR gate (b) 8-input NAND gate

Figure 0-20: Configuration of the eight-input OR and NAND gates

One main problem of logic gates is the propagation delay. In reality, the finite propagation delay from one logic block to the next can cause spurious transitions, including glitches, critical races and dynamic hazards. However, in the proposed digital-to-time converter, the input signals are the thermometer codes, which cannot change in the same time as long as the total propagation delay is smaller than the resolution of the delay chain. Moreover, only the change of the first and last channels will contribute to the propagation delay time. Table 4-4 shows the simulated low-to-high and high-to-low delays for different input patterns. According to the simulation results, the total propagation delay time of the digital-to-time converter is less than $1ns$

Table 0-4: Simulation delay times of the logic gates

Block	Logic change	Propagation delay time
OR	$0 \rightarrow 1$	$465ps$
	$1 \rightarrow 0$	$320ps$
NAND	$1 \rightarrow 0$	$265ps$
	$0 \rightarrow 1$	$365ps$
D flip-flop	$1 \rightarrow 0$	$349ps$
	$0 \rightarrow 1$	$269ps$
Total DTC	$0 \rightarrow 1$	$880ps$
	$1 \rightarrow 0$	$925ps$

1.16.3.6 Power estimation

Once all the main blocks of the modulator are designed, a transient simulation in Spectre has been run to estimate the power consumption. For the calculation we take in account blocks, including a Gm-C integrator, a continuous time comparator with internal hysteresis, a poly-phase sampler and a digital-to-time converter. Table 4-5 shows the bias current and equivalent estimated power consumption of each block in the proposed modulator.

Table 0-5: Estimation of power consumption of the proposed ASDM

Block	Bias current	Power consumption
Gm-C integrator	$10\mu A$	$200\mu W$
Comparator	$5\mu A$	$60\mu W$
Poly-phase sampler(delay chain)	$4\mu A$	$50\mu W$
Digital-to-time converter		$250\mu W$

1.16.3.7 Transistor-level simulation

A full SPICE transistor-level simulation of the proposed ASDM is taken in Spectre of Cadence. The sample frequency is set to be 2MHz, and it is divided by a delay chain with length of 8. The input tone is set to be one third of the analogue bandwidth, where the third order harmonic distortion is within signal bandwidth. The amplitude of the tone is $200mV$, and the equivalent normalized input amplitude V is 0.7.

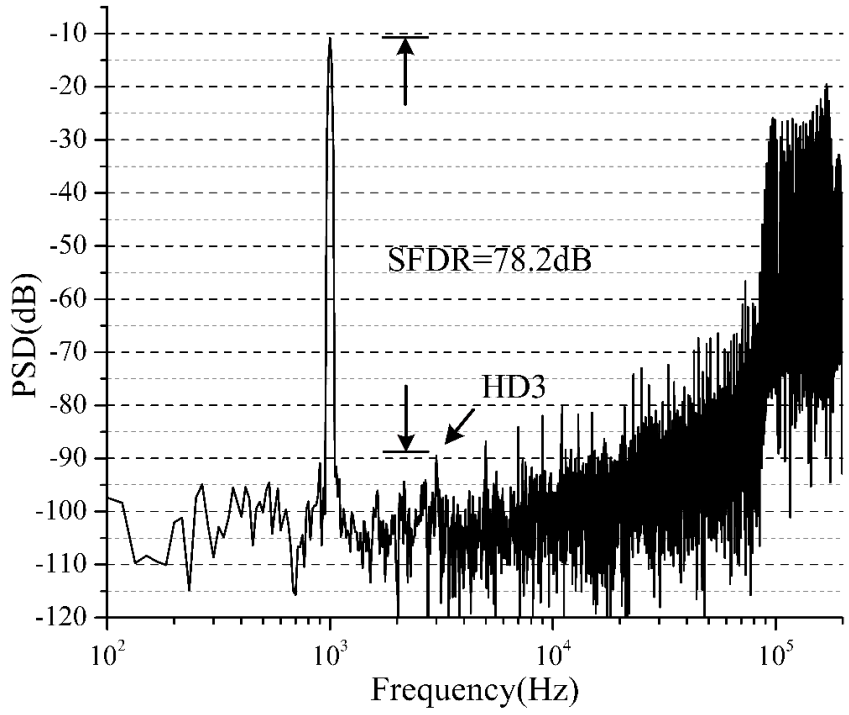


Figure 0-21: PSD of the proposed ASDM with input tone of one third of analogue bandwidth

Fig. 4-21 shows the PSD of the proposed ASDM with transistor-level simulation. Compared with PSD of the conventional ASDM (in Chapter 3), the proposed ASDM does have the first order

noise shaping. The SNDR of the modulator is 78.2dB, as expected, which is limited by the third order harmonic distortion.

1.17 Summary

In this chapter, the conventional solution to implement noise shaping in asynchronous sigma delta modulators has been discussed. By adding an additional loop filter and a multi-bit DAC, noise shaping is added into asynchronous sigma delta modulators. However, it is not a recommend solution, because it not only occupies a very large chip area and high power consumption, but also suffers many non-ideal effects, such as stability, non-linearity and clock jitter in multi-bit DAC.

To solve these issues, a novel asynchronous sigma delta modulator with noise shaping has been presented. The sampler is applied after the comparator, and feedback loop is realized by the digital-to-time converter. This novel modulator still belongs to asynchronous class, since the decision of the comparator is still determined by the input signal amplitude and not the clock. The proposed modulator is sampled by a 2MHz clock divided by an 8-stage delay chain. According to the simulation performed with the Spectre simulator of Cadence, the proposed modulator can achieved peak SNDR of 78.2dB, which is 22dB better than the conventional asynchronous sigma delta modulator with same sampling frequency.

The Asynchronous Sigma Delta Modulator with Constant Frequency

1.18 Introduction

Chapter 2 analysed the system characteristics of asynchronous sigma delta modulators, and both output frequency and the duty cycle were shown to be related to the input signal amplitude. Because of the variation of the output frequency, the limit cycle components shift to the baseband as shown in Fig. 5-1, and a high order filter with a high attenuation out of the pass band is required to maintain the resolution. In some low power application, limited performance of the filter limits the signal bandwidth of the modulator, because the limit cycle frequency needs to be moved far away from the baseband. In this chapter, a new solution to the frequency variation with input signal amplitude issue is presented.

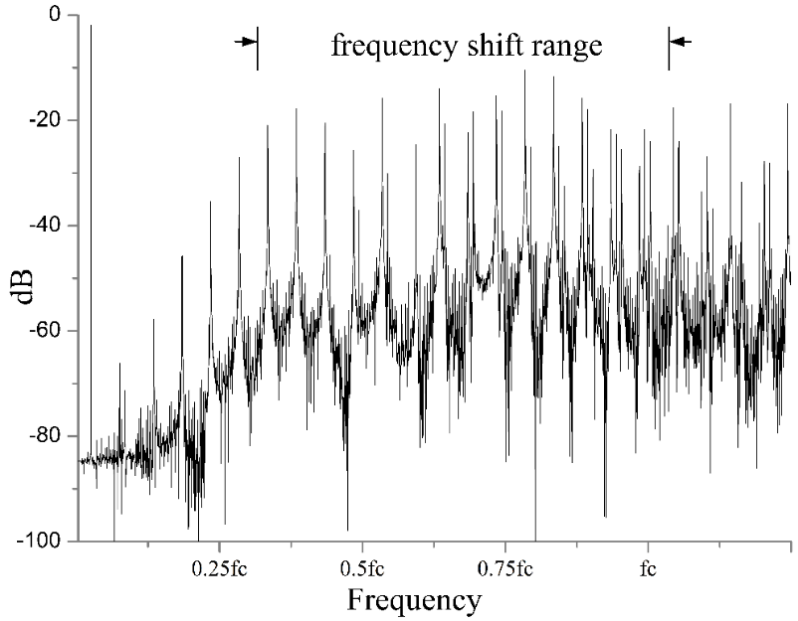


Figure 0-1: Limit cycle components of asynchronous sigma delta modulators

1.19 Asynchronous sigma delta modulators with delay cell

To begin with, we introduce another version of asynchronous sigma delta modulator as shown in Fig. 5-2 (a), where the comparator with hysteresis is replaced by a comparator and a delay cell is introduced in the feedback loop [44]. The delay cell can also been moved to the feed-forward loop as shown in Fig. 5-2 (b) and (c).

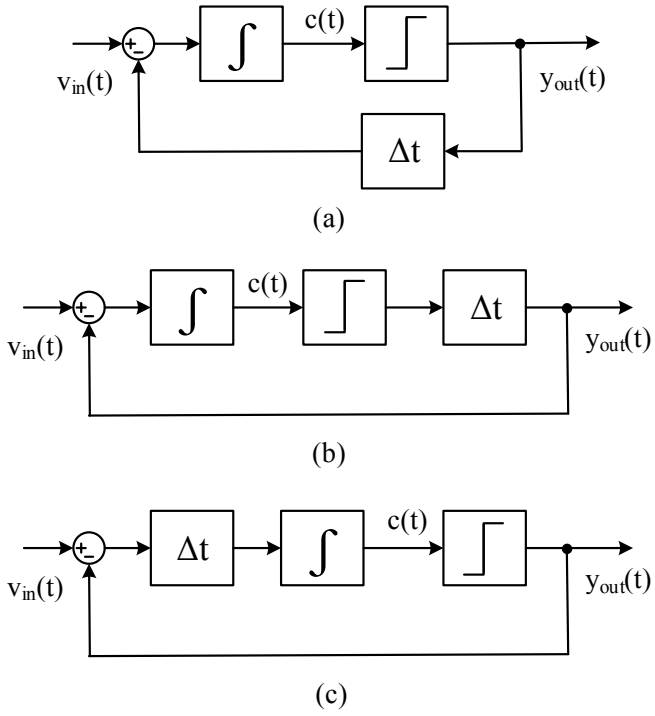


Figure 0-2: Configurations of asynchronous sigma delta modulator (a) the delay cell in the feedback loop [44]; (b) and (c) the delay cell in the feed-forward loop

Assuming there is a constant input signal $|V|<1$ is applied, the timing diagram is shown in Fig. 5-3. According to the timing diagram, the positive and negative time interval T_1 and T_2 can be described as:

$$T_1[n]=\Delta t_0-\frac{-1+V}{1+V}\Delta t_0 \tag{5-1}$$

$$T_2[n]=\Delta t_0-\frac{1+V}{-1+V}\Delta t_0 \tag{5-2}$$

Where Δt_0 is the delay time.

The output instantaneous frequency is:

$$f_{out} = \frac{1}{T_1 + T_2} = \frac{4}{\left(1 - V^2\right)\Delta t_0} \tag{5-3}$$

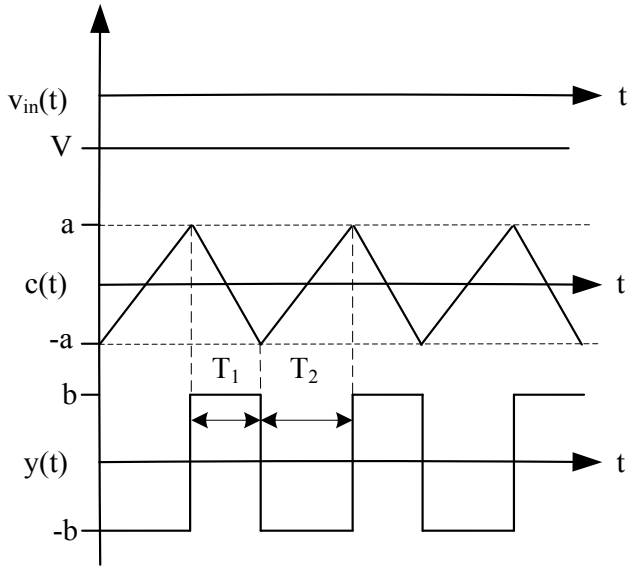


Figure 0-3: Timing diagram of the proposed asynchronous sigma delta modulator

When $V = 0$, the limit cycle frequency is

$$f_c = \frac{1}{4\Delta t_0} \tag{5-4}$$

With a sine wave input signal, the analysis is similar with that in Chapter 2. Assuming the input is $v_m \cos \mu t$, the output of loop filter can be described as:

$$\begin{aligned} c(t) = &\left[v_m \cos \mu (t - \Delta t) - (2\alpha - 1)_{t-\Delta t} \right] F(\mu) \\ &- \sum_{n=1}^{\infty} \frac{4}{n\pi} F(n\omega_i) \sin \alpha n\pi \cos\left[\alpha n\pi - n\omega_i (t - \Delta t) \right] \end{aligned} \tag{5-5}$$

The boundary conditions are:

$$\begin{cases} c(t) = 0 & at \quad t = T_1 + kT_k \\ c(t) = 0 & at \quad t = kT_k \end{cases} \tag{5-6}$$

Inserting eq. (5-6) to eq. (5-5) conditions will result:

$$\begin{aligned} c(t) = &\left[v_m - (2\alpha - 1) \right] F(\mu) \cos \mu (t - \Delta t) \\ &- \sum_{n=1}^{\infty} \frac{4}{n\pi} F(n\omega_i) \sin \alpha n\pi \cos \left[\alpha n\pi - n\omega_i (t - \Delta t) \right] \end{aligned} \tag{5-7}$$

Here we consider $\mu \Delta t << 1$ and use the same approximation implemented in chapter 2:

$$\mu (T_1 + kT_k) = 2\alpha\pi \frac{\mu}{\omega_i} + k\mu T_k \approx k\mu T_k = \mu T << 1 \tag{5-8}$$

and

$$\cos \mu (T_1 + kT_k) \approx \cos \mu k T_k \approx 1 \tag{5-9}$$

Based on the conditions (5-6), two equations can be obtained:

$$v_m - (2\alpha - 1) \approx \sum_{n=1}^{\infty} \frac{2}{n\pi} \mathrm{Re} \left(\frac{F(n\omega_i)}{F(\mu)} \right) \sin n\omega_i T_1 \cos \left(\frac{n\pi}{2} \cdot \frac{\omega_i}{\omega_0} \right) \tag{5-10}$$

$$\begin{aligned} &\sum_{n=1}^{\infty} \frac{4}{n\pi} \frac{F(n\omega_i)}{F(\mu)} \sin^2 \alpha n\pi \sin \left(\frac{n\pi}{2} \cdot \frac{\omega_i}{\omega_0} \right) \\ &= \left[v_m - (2\alpha - 1) \right] \sin \mu \left(\frac{T_1}{2} + kT_k - \Delta t \right) \sin \mu \frac{T_1}{2} \end{aligned} \tag{5-11}$$

It is clear to see that eq. (5-10) is very similar to eq. 2-16 in Chapter 2. As long as the variation of the input signal is slow, the duty cycle of the modulator is proportional to the input amplitude.

Compared with the conversional asynchronous sigma delta modulator (Fig. 2-8(a)), there are some disadvantages in the proposed configuration. Because of the absence hysteresis in the comparator, the comparator is sensitive to the noise. Another disadvantage is that this configuration is sensitive to the delay in the loop. The finite open loop gain and slew rate of amplifiers used in the loop filter and comparator will increase propagation delay time of the system, which will decrease the limit cycle frequency. The main challenge for this kind of configuration is require a high linear performance delay line.

However, there are many attractive features of this kind of configuration. The main advantage is that it can stabilise the output frequency by controlling the delay time of the delay cell. Another one is that the limit cycle frequency of the proposed configuration depends on the delay cell. Theoretically, the variation of loop filter factor (RC) will not affect the limit cycle frequency. More details are given in the next section.

1.20 The proposed asynchronous sigma delta modulator

1.20.1 Frequency compensation

The frequency compensation is realized by controlling the delay time of the delay cell. By implementing the voltage (current) controlled delay line, the delay time can be set to be a different value in different conditions. Assuming $\Delta t_n[n]$ is the delay time when the feedback is negative in N^{th} period; and $\Delta t_p[n]$ is the delay time when the feedback is positive, eq. (5-1) and (5-2) can be rewritten as:

$$T_1[n] = \Delta t_p[n] - \frac{-1+V}{1+V}\Delta t_n[n-1] \tag{5-12}$$

$$T_2[n] = \Delta t_n[n] - \frac{1+V}{-1+V}\Delta t_p[n] \tag{5-13}$$

The delay times are controlled by the input signal amplitude. The period of N^{th} cycle can be described as:

$$T[n] = T_1[n] + T_2[n] \approx \frac{-2}{-1+V}\Delta_p[n] + \frac{2}{1+V}\Delta_n[n] \tag{5-14}$$

When the variation of the input signal is much slower than the limit cycle frequency $\Delta t_n[n-1]$ is approximately equal to $\Delta t_n[n]$. Based on the equation above, the compensation coefficients can be identified as:

$$\begin{cases} k_n = \eta(1+V) \\ k_p = -\eta(-1+V) \end{cases} \tag{5-15}$$

By inserting the coefficients to the eq. (5-14), the period of N^{th} cycle is

$$T[n] = 4\eta\Delta t \tag{5-16}$$

Eq. (2-24) can be rewritten as:

$$y_1(t) = \mathrm{Re}\frac{4}{\pi}\sum_{n=-\infty}^{\infty} J_n\left(\frac{\pi}{2}V\right)e^{in(\pi/2-\mu t+\omega_0 t)} \tag{5-17}$$

And the duty cycle can be represented as:

$$\alpha[n] = \frac{T_1[n]}{T[n]} = \frac{k_p\Delta t_0 - \frac{-1+V}{1+V}k_n\Delta t_0}{\frac{-2}{-1+V}k_p\Delta t_0 + \frac{2}{1+V}k_n\Delta t_0} = \frac{1-V}{2} = \frac{1+|V|}{2} \tag{5-18}$$

Obviously, the compensation will not change the basic duty cycle characteristic of asynchronous sigma delta modulator.

The distortion of the proposed ASDM with first order loop filter can be described as:

$$\Delta_3 = \frac{\pi^2}{24} \cdot \frac{\mu^2 + p_1^2}{\omega_c^2 + p_1^2} V^2 \tag{5-19}$$

Where ω_c is the limit cycle frequency, p_1 is the pole frequency of the integrator filter.

The comparison of SFDR between the conventional and proposed ASDMs with first order loop filters is shown in Fig. 5-4, where the pole frequency of the loop filter is set to be equal to the input signal frequency. It is clear that with the benefits of the frequency compensation, the SFDR of the proposed ASDM drops less than the conventional one at large input signal. This is because the total number of the limit cycle components is reduced and they do not shift to the baseband. Assuming the output is filtered by an ideal low pass filter, the SFDR for the proposed one can be improved to 10dB with the maximum input amplitude.

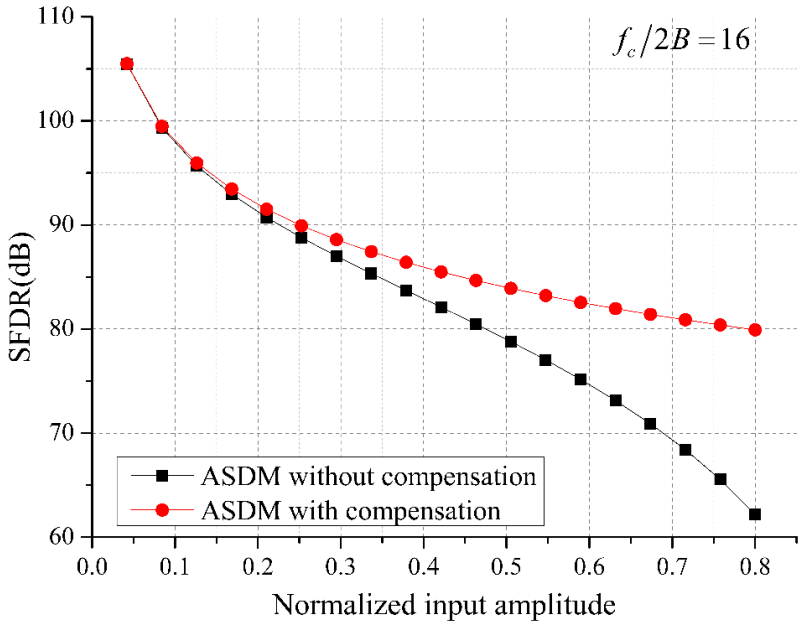


Figure 0-4: SFDR of the conventional and proposed 1st order ASDMs versus normalized input amplitude ($p_0/2\pi = f_{in} = B/3$)

In addition, the requirement of carrier-to-bandwidth ratio for the proposed ASDM is reduced. For the worst case, when the normalized input amplitude is 0.8, the estimation of SFDR versus carrier-to-bandwidth ratio is shown in Fig. 5-5. Note that for the proposed ASDM, the requirement of the

carrier-to-bandwidth ratio is reduced to 16 to obtain the SFDR over 70dB. In other words, the proposed ASDM can obtain a wider signal bandwidth with the same carrier-to-bandwidth ratio.

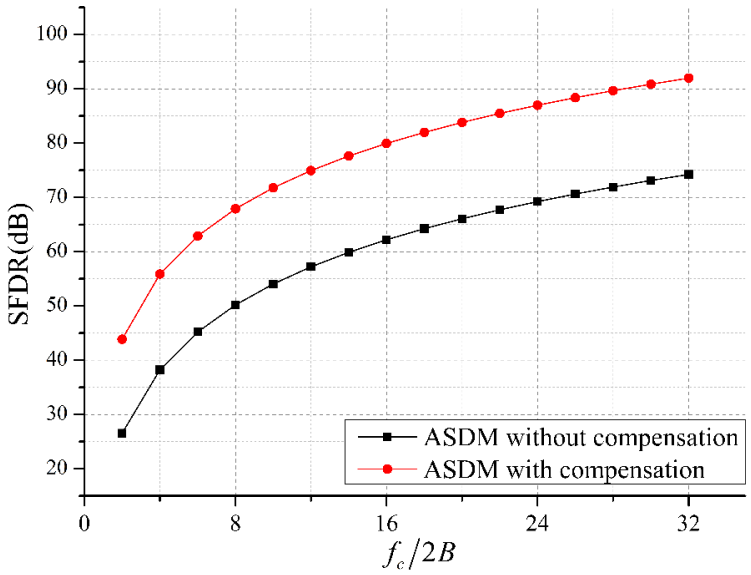


Figure 0-5: Estimation for achieved SFDR versus $f_c/2B$ ($V=0.8$ and $p_1/2\pi = f_{in} = B/3$)

1.20.2 Non-ideal effects

According to eq. (5-15), the values of two coefficients are $1 \pm V$, which are equal to absolute value the input of the integrator during different phases. In order to avoid using rectification circuits, the proposed compensation configuration is shown in Fig. 5-6. The principle of the compensation scheme is very simple: two switches are controlled by the feedback signal so as to generate relative control voltages for the delay cell. When input is non-zero, assuming V_{in} for example, the operation can be divided into two phases:

- Phase one: the feedback is positive. In that case, the switch k_1 is open and k_2 is closed. The delay controlled voltage is changed to $-V_{in}$, and consequently, the delay time is equal to $\Delta t_0 + \Delta t\left(-V_{in}\right)$.
- Phase two: the negative feedback is negative, and under that condition, k_1 is closed and k_2 is open, and the delay will be $\Delta t_0 + \Delta t\left(V_{in}\right)$.

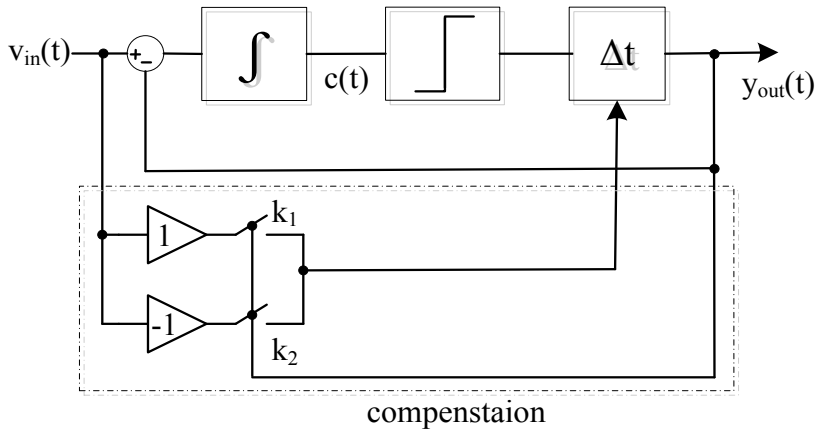


Figure 0-6: System diagram of the first-order asynchronous sigma delta modulator with frequency compensation

In a practical implement, $\pm V_{in}$ can be easily obtained by using full differential architecture. In rest of this section, the issues of analogue imperfections in several building blocks of the proposed ASDM will be analysed.

1.20.2.1 Non-linear performance of the delay cell

The compensation of the proposed ASDM mainly depends on the source controlled delay line. The linear performance of the delay cell will significantly affect the accurate of the compensation. Assuming the non-linear errors occurred in the delay cell are $\varepsilon_n \Delta t_0$ and $\varepsilon_p \Delta t_0$ for Δt_n and Δt_p respectively. According to eq. (5-12) and eq. (5-13), the normalized input amplitude V is related to the output signal by:

$$V'[n] = \frac{T_1[n] - T_2[n]}{T_1[n] + T_2[n]} = \frac{2V[n] - \frac{1}{1+V[n]}\varepsilon_n + \frac{1}{1-V[n]}\varepsilon_p}{2 + \frac{1}{1+V[n]}\varepsilon_n + \frac{1}{1-V[n]}\varepsilon_p} \tag{5-20}$$

The worst case is that $\varepsilon_n = -\varepsilon_p = \varepsilon$ or $-\varepsilon_n = \varepsilon_p = \varepsilon$, hence non-linear error is:

$$V_{error} = \frac{\pm\varepsilon}{1 \pm \frac{V}{1-V^2}\varepsilon} \tag{5-21}$$

Obviously, the high resolution of the delay cell will increase the linear performance of the proposed ASDM. Fig. 5-8 shows the estimation of the worst non-linear errors of the proposed system versus normalized input amplitude as obtained from eq. (5-20) and from simulation. Note that high linear performance delay cell with at most 1% non-linear errors is required to maintain the linear performance of the ASDM.

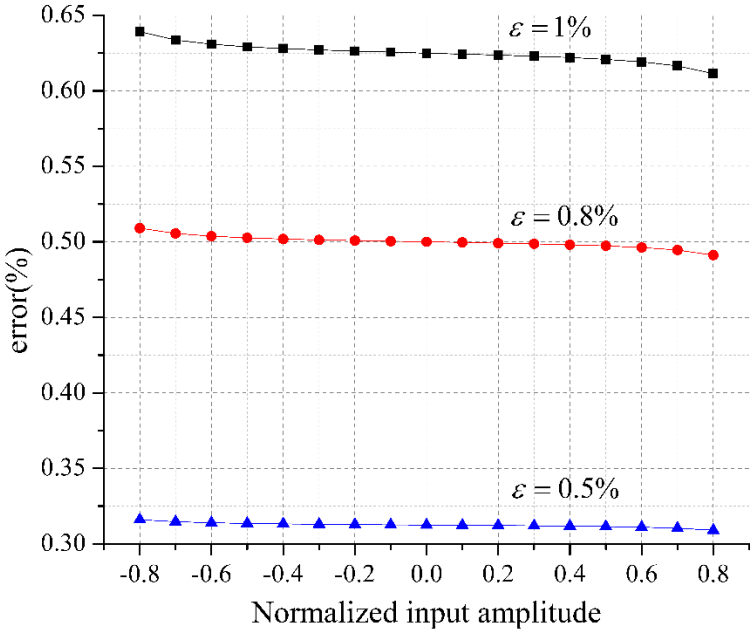


Figure 0-7: Errors versus normalized input amplitude and three different value of ε

Nonlinearities of the delay cell will shift the limit cycle frequency. However, based on eq. (5-20), the difference is so small that the frequency components will not shift near the baseband.

1.20.2.2 Propagation delay and hysteresis in non-ideal comparator

Because the limit cycle frequency of the proposed asynchronous sigma delta modulator mainly depends on the delay time, the effect of the propagation delay time is different than that for the conventional one. The propagation delay time in the proposed ASDM will introduce a limit on the limit cycle frequency, and will also limit the minimum compensation value:

$$f_c = \frac{1}{4\left(\Delta t_0 + t_p\right)} \geq \frac{1}{4t_p} \tag{5-22}$$

The estimation for achieved SFDR versus $t_p/\Delta t_0$ is shown in Fig. 5-8. Note that for $t_p/\Delta t_0 = 0.2$, the SFDR of the system will reduce to 73.8dB. Moreover, as this extra delay time will reduce the limit cycle frequency, the benefit of the compensation block will reduce. This is because the compensation only applies to the initial delay time, and do nothing for the extra delay time. In order to minimize this extra delay time, the comparator with a latch is required. More details are given in next section.

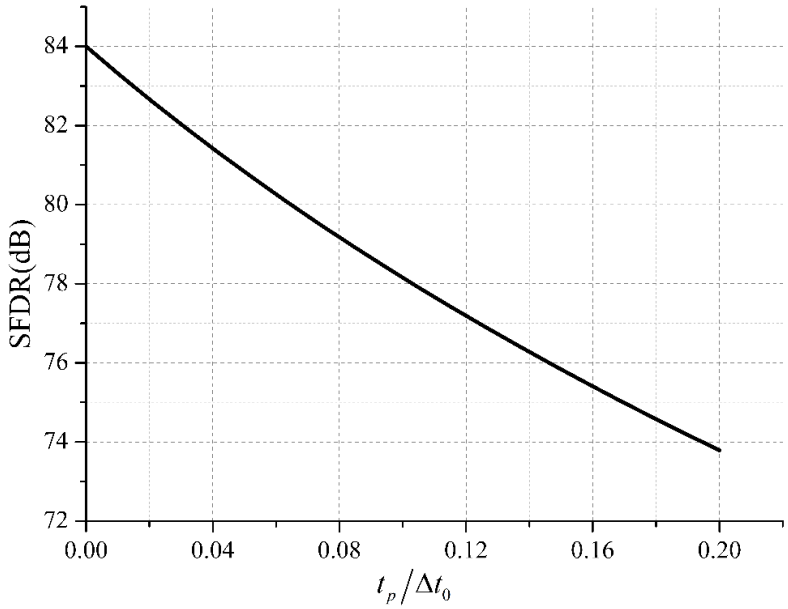


Figure 0-8: Estimation for achieved SFDR versus $t_p/\Delta t_0$ with $V = 0.8$ ($f_c/2B = 16$, $f_{in} = B/3$, $p_1/B = 1/6$)

Another issue of the comparator is existing the minimum input voltage $V_{in}(\min)$. This issue will not affect the conventional configuration, as comparator has hysteresis value normally several times large than $V_{in}(\min)$. The minimum input voltage of the comparator in the proposed asynchronous sigma delta modulator can be considered as effectively adding a small value hysteresis to the comparator. Therefore, we can here utilize the analysis of the conventional

asynchronous sigma delta modulator. Together with the integration gain ($k = 1/RC$), this threshold voltage will cause the generation of extra frequency components, the maximum one is:

$$f_{extra} = \frac{k}{4V_{in}(\min)} \tag{5-23}$$

For example, assuming a non-ideal comparator with output swing voltage of $\pm 0.6V$ and DC gain of 60dB. The minimum input voltage is about $\pm 0.6mV$. Here we set the limit cycle frequency to 200kHz, and choose the suitable integration gain, the maximum extra frequency component is over 100MHz, which will slightly affect the baseband signal.

Another drawback of the proposed configuration is that the comparator is sensitive to the noise. If the comparator is fast enough (depending on the frequency of the most prevalent noise) and the amplitude of the noise is great enough, the noise will lead to an uncertainly in the transition region, which in turn will lead to jitter or phase noise in the modulator. The traditional method around this issue is to add hysteresis in the comparator. However, similar to the minimum input voltage, introduction of hysteresis will generate extra frequency components. Assuming the hysteresis is b ($|b| < 1$), the output frequency becomes:

$$f_c' = \frac{1}{4\Delta t_0 + \frac{2b}{\beta(1-m^2)}} \tag{5-24}$$

Note that by increasing the integrator factor, this effect can be minimized. However, the integrator factor is limited by the performance of the amplifier/tranconductor and charging/discharging capacitance. A large integration gain (1/RC value) requires a small resistor/large tranconductance and a small capacitance, which significantly increases the power consumption and noise floor. The estimate of this effect versus integration gain is shown in Fig. 5-9, where the normalized hysteresis $b = 0.1$. In order to maintain SFDR over 75dB, the integrator factor (1/RC) need to be over 1.5×10^5. A way to solve this issue is to add an extra gain stage between the loop filter and the comparator. Eq. (5-24) can be rewritten:

$$f_c' = \frac{1}{4\Delta t_0 + \dfrac{2b}{A_0\beta\left(1-m^2\right)}} \tag{5-25}$$

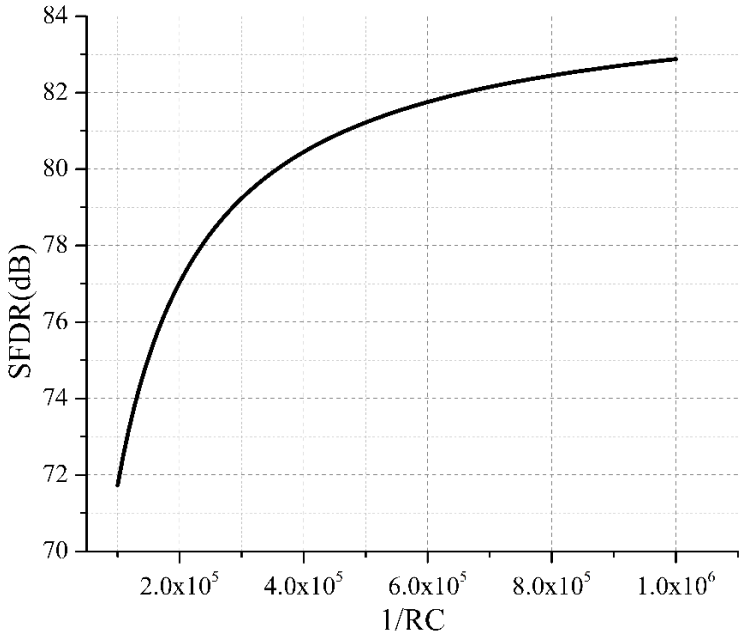


Figure 0-9: Estimation for achieved SFDR versus integrator factor ($f_c/2B = 16$, $p_0/B = 1/6$ $f_{in} = B/3$ and $b = 0.1$)

There are two advantages of this gain stage. One is it reduces the requirement of the integration gain. The other one is it increases the over drive voltage of the comparator, which can reduce the propagation delay time.

The PSD of the proposed configuration is shown in Fig. 5-10, when the comparator of the ASDM is built without noise ((a)) and with a relative noise ((b), (c), and (d)). The carrier-to-bandwidth ratio is 16, and the output is sampled by a 100MHz clock. The in-band noise floor of the proposed modulator is below -85dB when there is no noise added to the comparator (Fig. 5-10 (a)). By adding white noise to the comparator, as expected, the noise floor increases to -55dB (Fig. 5-10 (b)). In Fig. 5-10 (c), a normalized hysteresis $b = 0.1$ is applied to the comparator, the in-band noise floor is below -67dB. However, this hysteresis does increase the distortion of the modulator, the third order harmonic distortion increases from -85dB to -64dB. By adding a gain stage ($A_0 = 10$)

before the comparator, the in-band noise floor reduced to -79dB, and the third order harmonic distortion also is reduced to -77dB. These finding support the analysis we introduced previously.

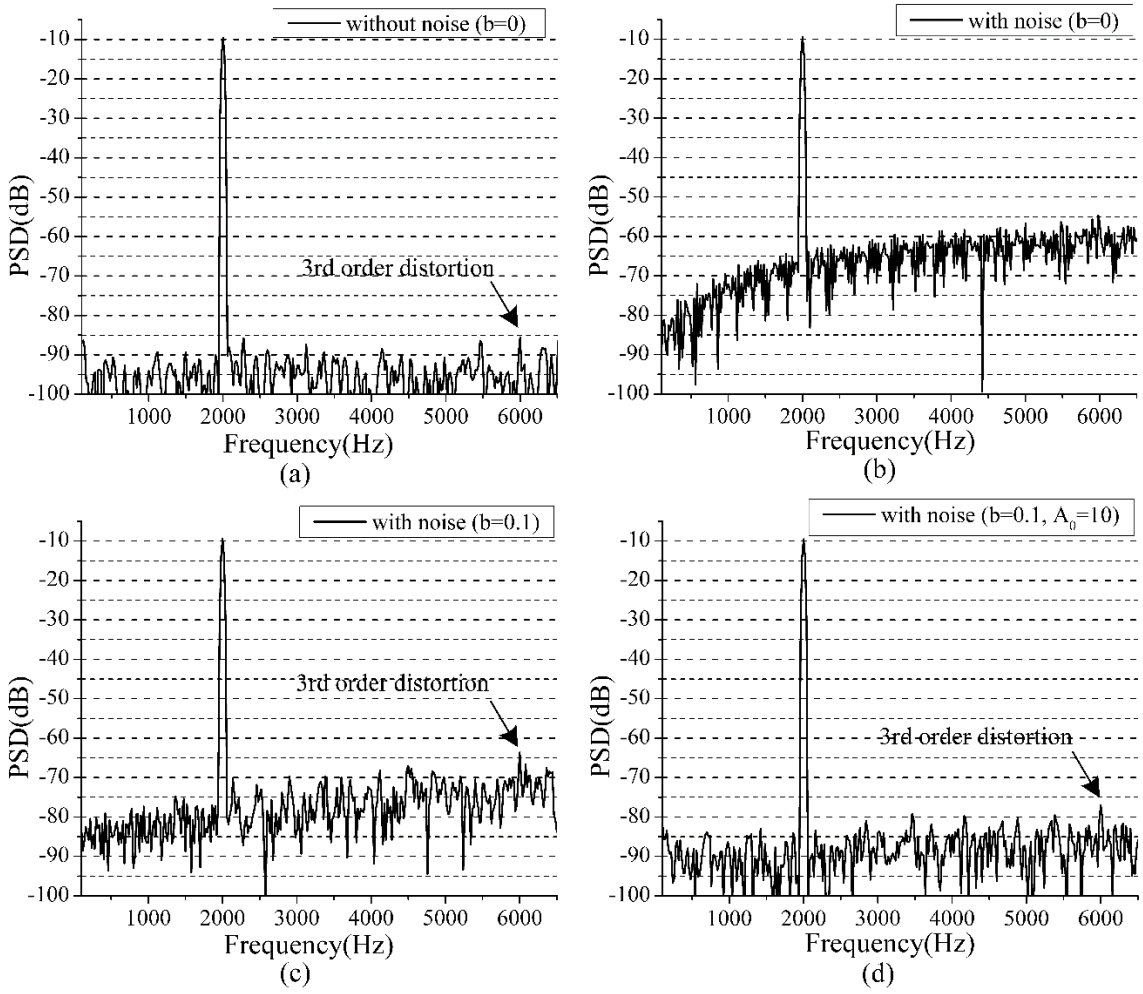


Figure 0-10: PSD for the proposed ASDM: (a) without noise, (b) with noise and $b=0$, (c) $b=0.1$, (d) $b=0.1$ and $A_0=10$ ($f_s=100MHz$)

1.20.2.3 Non-ideal loop filter

As shown in Chapter 2, the pole location of the loop filter will affect the SFDR of ASDMs. Fig. 5-11 shows the SFDR versus the pole of the loop filter for the proposed ASDM. Similar to the conventional ASDM, the proposed one is also sensitive to the pole of the loop filter. According to Fig. 5-11, the SFDR will reduce approximate 20dB, when the pole of the loop filter is equal to the signal bandwidth.

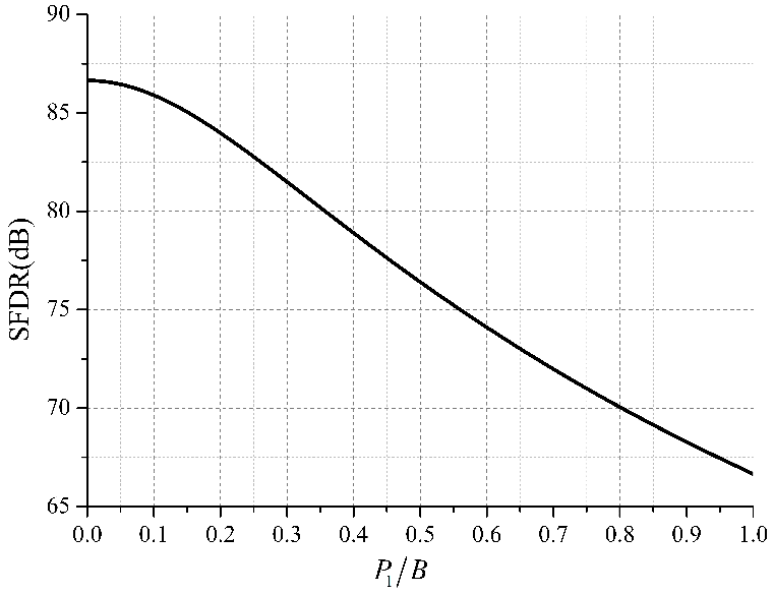


Figure 0-11: SFDR versus the pole of the loop filter ($f_c/2B=16$)

Another different between the conventional ASDM and proposed configuration is that the behaviour of the later one has no relationship with the value of the integration gain in theory. And on order to minimize the propagation loop delay of the comparator, the integration gain should be set as large as possible utile the delay time is limited by the slew rate of the comparator. While, in the practice, because of analogue block imperfections, the integration gain for the proposed ASDM is also limited by the hysteresis of the comparator as mentioned in the above and specifications of the amplifier. In the proposed ASDM, the output of the loop filter is:

$$c(\max)=\left[\beta\left(1-m^2\right)\Delta t_0+b\right]V_s \overset{m=0}{=} \left(\beta\Delta t_0+b\right)V_s \tag{5-26}$$

The integration gain should not be over:

$$\beta \le \frac{1-b}{\Delta t_0} \tag{5-27}$$

The proposed ASDM is insensitive to the variation of the integration gain, causing by variation of resistors, capacitors or Gm-cells implemented in the integrator. Fig. 5-12 shows the estimation

SFDR versus variation index of the integration gain. Note that the SFDR of the modulator only dropped $0.8dB$ when a 30% variation of the integration gain is applied.

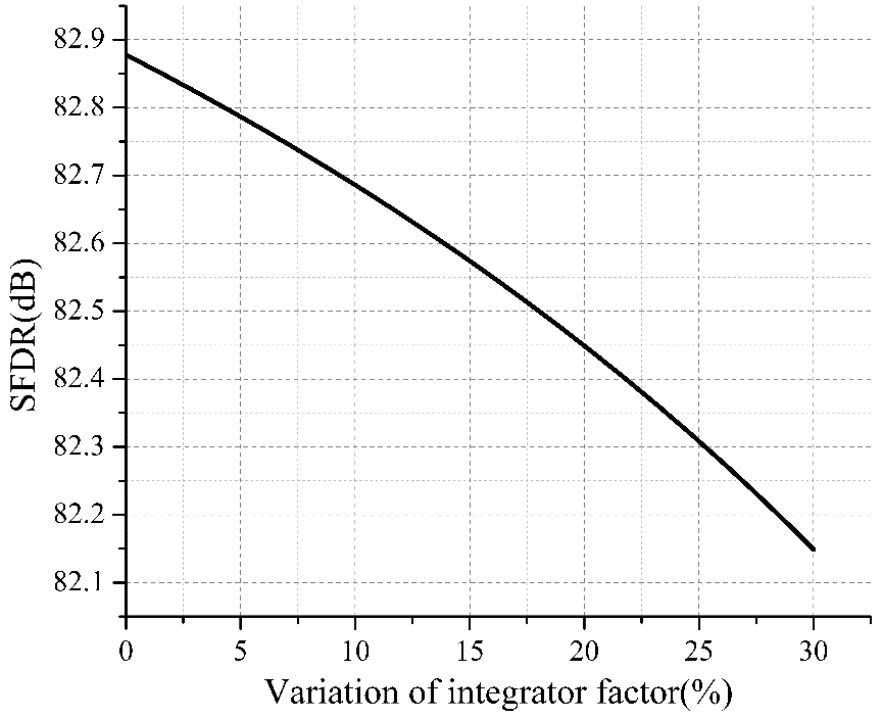


Figure 0-12: Estimation for achieved SFDR versus variation of integrator factor ($b = 0.1$, $f_c/2B = 16, V = 0.8$ and $f_{in} = B/3$)

1.20.3 SNDR comparison

In this section, a SNDR comparison is made between the conventional first-order ASDM and the proposed one, and the outputs are fed into an ideal third order Butterworth low pass filter with attenuation of 60dB at stop band. The loop filter is realized by active RC integrator, and the imperfections are listed in Table 5-1. The PSD of ASDMs are obtained by Simulink of Matlab as shown in Fig. 5-13. Fig. 5-13 (a) and (b) show the PSD of the conventional ASDM with 6kHz and 3kHz input signal.

Table 0-1: values of parameters in the simulation

Imperfections	Value
Limit cycle frequency f_c	200kHz
Signal bandwidth B	6kHz
Normalized input voltage V	0.8
Finite gain A_0	60dB
$-3dB$ bandwidth	300kHz
Pole of the integrator	2kHz
Propagation delay t	10ns
Delay cell non-linear performance	$<1\%$
Variation of integrator factor k	$<10\%$

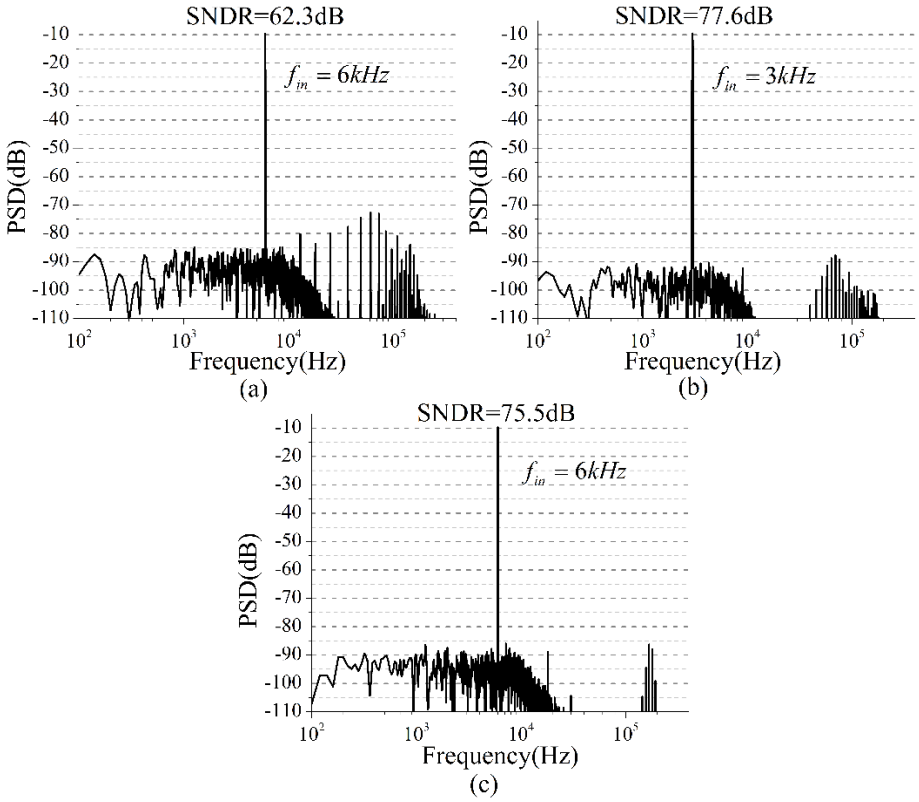


Figure 0-13: PSD of the conventional and proposed first-order asynchronous sigma delta modulators: (a) and (b) are the conventional ASDM with 6kHz and 3kHz inputs, respectively; (c) the proposed ASDM with 6kHz input

Because the limit cycle components shifts, the SNDR of the conventional ASDM drops from 77.6dB to 62.3dB, when the frequency of input signal is doubled. While for the proposed one (Fig. 5-13 (c)), the SNDR of 75.5dB is obtained when a 6kHz input signal is applied. Compared with the conventional one, the SNDR is improved by 12dB. In order words, with the same limit cycle frequency, the proposed ASDM can obtain wider signal bandwidth than the conventional one.

1.21 Circuits level design

The system diagram and parameters defined in the previous section are used as the start point of a CMOS circuit design. For this proof-of-concept circuit, a conservative $0.35\mu m$ standard CMOS process and a dual power supply of $\pm 1.5V$ are selected. The configuration of the proposed modulator is shown in Fig. 5-14.

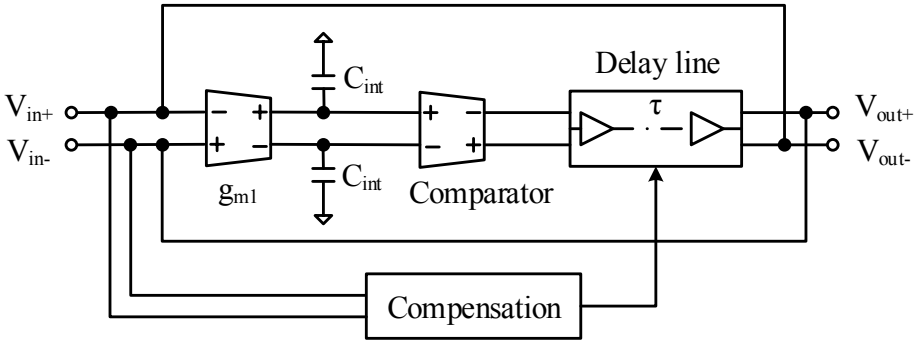


Figure 0-14: Configuration of the proposed modulator

1.21.1 Loop filter and comparator

The loop filter configuration loop filter implemented here is the same as that in Chapter 3. Since the tranconductance of the loop filter will not determine the limit cycle frequency, here we select a large tranconductance in order to minimize the pole frequency effect of the loop filter. The schematic of the comparator is shown in Fig. 5-15. And the size of transistors are listed in Table 5-2. The main performance of the comparator is shown in Table 5-3.

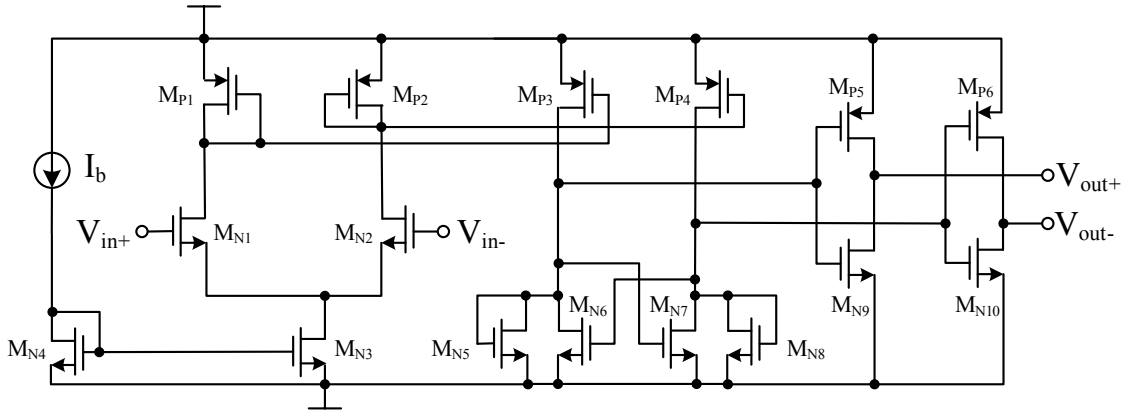


Figure 0-15: Schematic of the comparator implemented in the proposed modulator

Table 0-2: Sizes of transistors in the comparator

Transistor	Size (W/L)
M_{P1},M_{P2}	$6\mu m/1\mu m$
M_{P3},M_{P4}	$6\mu m/1\mu m$
M_{P5},M_{P6}	$6\mu m/1\mu m$
M_{N1},M_{N2}	$50\mu m/1\mu m$
M_{N3}	$8\mu m/2\mu m$
M_{N4}	$4\mu m/2\mu m$
M_{N5},M_{N6},M_{N7},M_{N8}	$2\mu m/20\mu m$
M_{N9},M_{N10}	$2\mu m/1\mu m$

Table 0-3: Main parameters of the comparator

Parameters	Performance
Supply voltage	$\pm 1.5V$
Bias current	$5\mu A$
Open loop gain	$52.5dB$
Bandwidth ($-3dB$)@ $0.5pF$	$300kHz$
Slew rate@ $0.5pF$	$80V/\mu s$
Propagation delay	$< 30ns$

1.21.2The proposed voltage controlled delay line (VCDL)

The compensation block configuration is shown in Fig. 5-16. The compensation block includes a voltage-to-current converter (VCC), a translinear loop (TL loop) and a delay line. By cascading VCC and TL loop, a linear transfer function for the voltage controlled delay line can be realized.

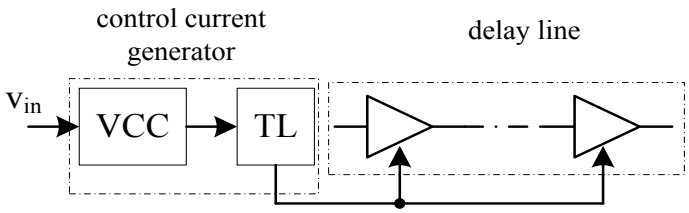


Figure 0-16: Configuration of the compensation block

1.21.2.1 Voltage-to-current converter and translinear loop

The schematic of the voltage-to-current converter is shown in Fig.5-17. In order to realize the highly linear performance, a passive resistor is implemented in the VCC. The other terminal of the resistor is connected to a signal ground node which is enforced by a high-gain negative feedback loop implemented by an amplifier A and transistors M_{N1} and M_{N3}. Due to this signal ground a highly linear V-I conversion takes place, the resistor current is:

$$I_{in} = \frac{V_{in} - V_{bias}}{R} \tag{5-28}$$

This current is conveyed to the high impedance output node by the cascade current mirror formed by transistors M_{N1}, M_{N2}, M_{N3} and M_{N4}. Finally, this current is accurately copied to output current through the upper PMOS cascade current mirror formed by transistors M_{P7}, M_{P8}, M_{P9} and M_{P10}. The output current can be derived as:

$$I_x = N_1 N_2 \left(I_{bias} + \frac{V_{in}}{R} \right) \tag{5-29}$$

Where N_1 is the ratio between the W/L of M_{N2} and M_{N5}; N_2 is the ratio between $M_{P7}$and M_{P8}, here $N_1 = (W/L)_{M_{N1}} = (W/L)_{M_{N2}}$, $N_2 = (W/L)_{M_{P2}} = (W/L)_{M_{P5}}$.

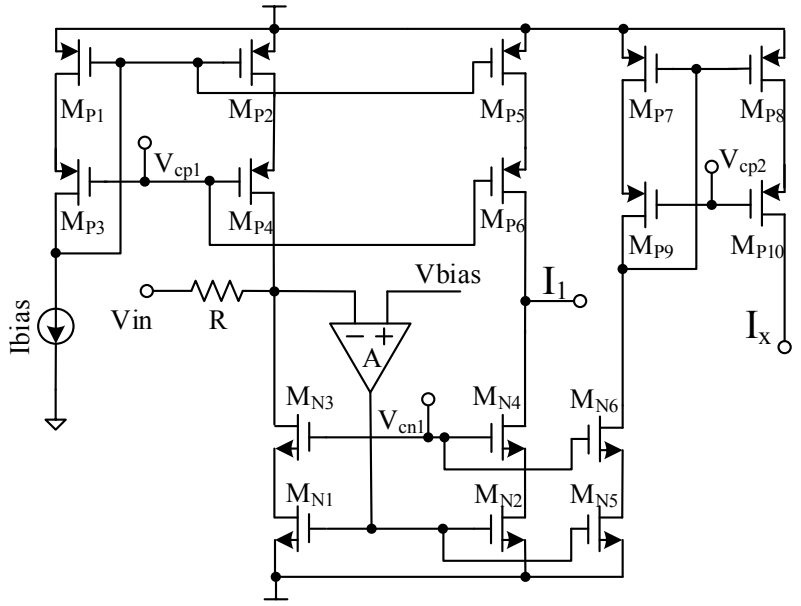


Figure 0-17: Schematic of the voltage-to-current converter

The amplifier schematic is shown in Fig. 5-18. Here a conventional folded cascode amplifier is implemented to realize a high open loop gain. The sizes of all transistors in the voltage-to-current converter is listed in the Table 5-4.

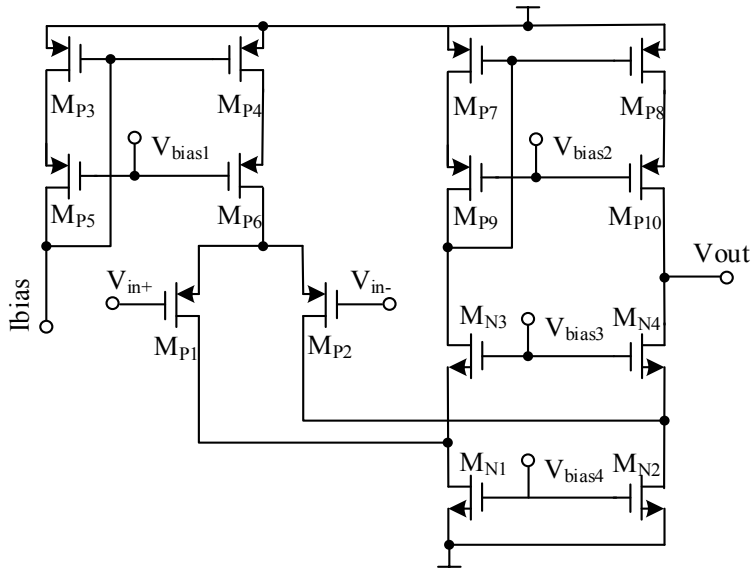


Figure 0-18: Schematic of the amplifier in the VCC

Table 0-4: Sizes of transistors in the voltage-to-current converter

Voltage-to-current converter	
Transistors	W/L
M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_{P5}, M_{P6}	$8\mu m/2\mu m$
M_{N1}, M_{N2}, M_{N3}, M_{N4}	$4\mu m/2\mu m$
M_{N5}, M_{N6}	$2\mu m/2\mu m$
M_{P7}, M_{P8}, M_{P9}, M_{P10}	$4\mu m/2\mu m$
Folded cascode amplifier	
M_{P1}, M_{P2}	$10\mu m/1\mu m$
M_{P3}, M_{P4}, M_{P5}, M_{P6}	$8\mu m/2\mu m$
M_{P7}, M_{P8}, M_{P9}, M_{P10}	$4\mu m/2\mu m$
M_{N1}, M_{N2}	$2\mu m/2\mu m$
M_{N3}, M_{N4}	$4\mu m/2\mu m$

The voltage-to-current converter using a passive input resistor connected to a signal ground not only to improve the linear performance, but also to realize rail-to-rail input operation. In fact, input swing is limited by the driving stage. The main drawback of this class-A voltage-to-current converter is that the input impedance is limited by the product of open loop gain of the amplifier and transconductance of the resistor M_{N1}, which cannot be very large if a large open gain is applied. Indeed, the output current is limited by the bias current I_{bias}. This represents a trade-off between static power consumption and input/output current swing. While this will not be an issue in the proposed ASDM, this is because the initial delay time of the delay cell is determined by this bias current.

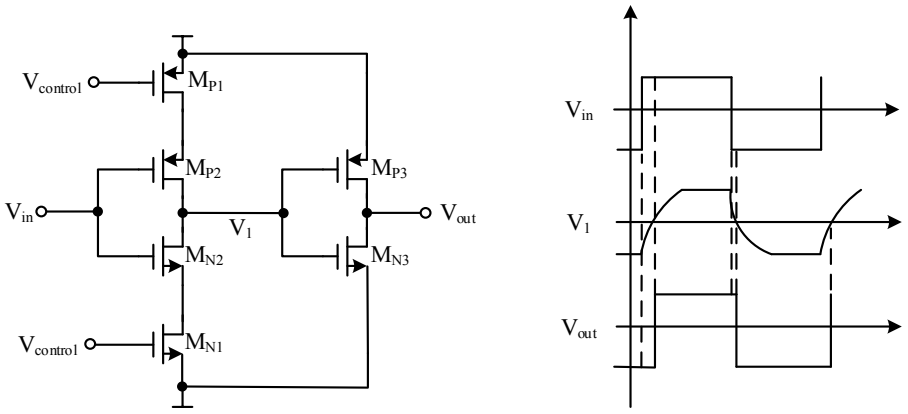
The same architecture that was used in Chapter 3 is implemented here in the translinear loop. According to the translinear principle, the output current of the TL loop can be described as:

$$I_y = \frac{I_0^{\,2}}{I_x} = \frac{I_0^{\,2}}{N_1 N_2 \left(I_{bias} + \frac{V_{in}}{R} \right)} \tag{5-30}$$

Where I_0 is the bias current in TL loop.

1.21.2.2 Delay cell

The delay elements implemented in the proposed circuit are slightly different than conventional ones, where the delay time for rising and falling edges should be equal. In practice, there will be some stretching or shrink phenomenon in delay lines, as shown in Fig. 5-19. Because of the difference between charging and discharge time of the capacitor, the pulse of the input square wave is compress by a delay cell. In order to minimize this mismatch, a small RC value is required, where the slopes of charging and discharging phases can be considered to be approximately equal. Here we cascade several delay cells with small delay time to obtain the required delay time, as shown in Fig 5-20.



(a) (b)

Figure 0-19: Shrinking/Stretching for the delay line: (a) Schematic of conventional delay cells; (b) Timing diagram

Two delay elements are cascaded in the proposed delay lines. Each of the delay cell implements the current starving technology, which is designed for a symmetric slew rate in order to minimize the mismatch between the rising and falling edges. Together with the VCC and TL loop, the delay time of the delay line can be derived as:

$$\Delta t = \frac{CV_{sw}}{I_0^{\,2}} R_1 R_2 \left(I_{bias} + \frac{V_{in}}{R} \right) = \beta \left(I_{bias} + \frac{V_{in}}{R} \right) = \Delta t_0 + \frac{\beta V_{in}}{R} \qquad (5\text{-}31)$$

Where $\Delta t_0 = \beta I_{bias}$, $\beta = R_1 R_2 \, CV_{sw} / I_0^{\,2}$ is the design coefficient.

Based on the equation above, the compensation can be realized, and the delay times of two phases are:

$$\begin{cases} \Delta t_p = \beta \cdot \left(I_{bias} - \dfrac{V_{in}}{R} \right) \propto (1 - V)\Delta t_0 \\ \Delta t_n = \beta \cdot \left(I_{bias} + \dfrac{V_{in}}{R} \right) \propto (1 + V)\Delta t_0 \end{cases} \tag{5-32}$$

The transistor sizes are shown in Table 5-5. In order to minimize the effect of the mismatch and process variation, a large transistor size ($W \times L$) is chosen.

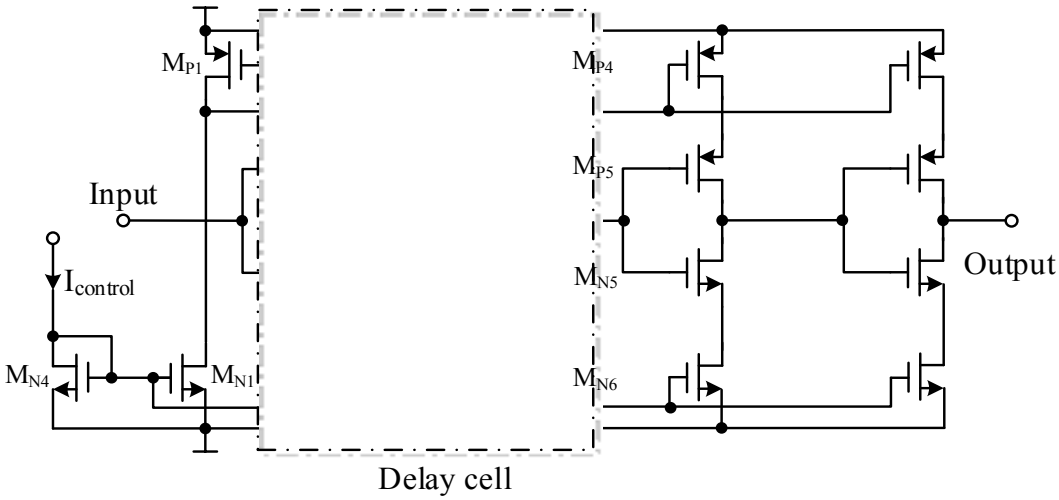


Figure 0-20: Schematic of the proposed delay line by cascading two delay cells

Table 0-5: Sizes of the transistors in the delay element

Transistors	W/L
M_{N1}, M_{N2}, M_{N4}, M_{N6}	$4\mu m/2\mu m$
M_{N3}, M_{N5}	$2\mu m/1\mu m$
M_{P1}, M_{P2}, M_{P4}	$6\mu m/2\mu m$
M_{P3}, M_{P5}	$5\mu m/1\mu m$

1.21.2.3 Simulation

The main issue in this block is compression and expansion of the pulse width. Based on the simulation, the mismatch between the rising and falling phases is within 4ns for full range, as

shown in Fig. 5-21. And by applying a square wave with duty cycle of 50%, the error caused by the compression and expansion versus control voltage is shown in Fig. 5-22. For full range variation, the normalized error is within 0.2%.

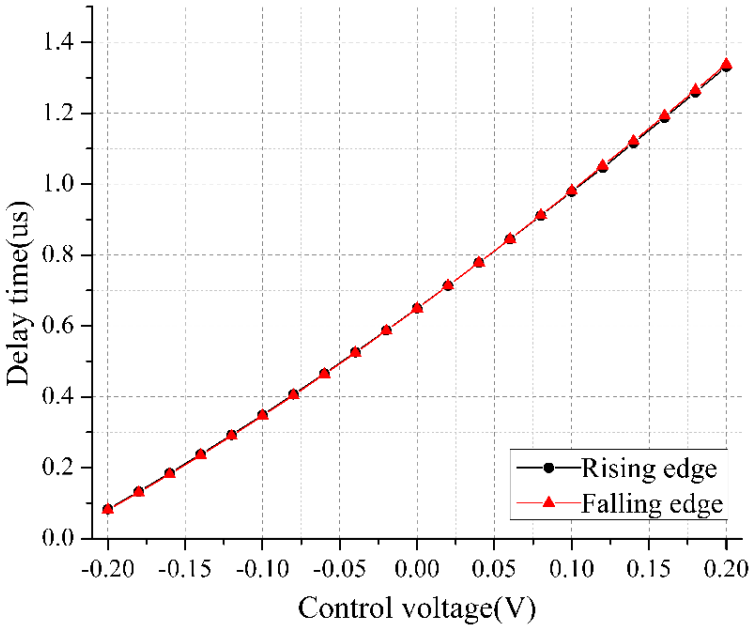


Figure 0-21: Delay time of the rising and falling phase versus control voltage

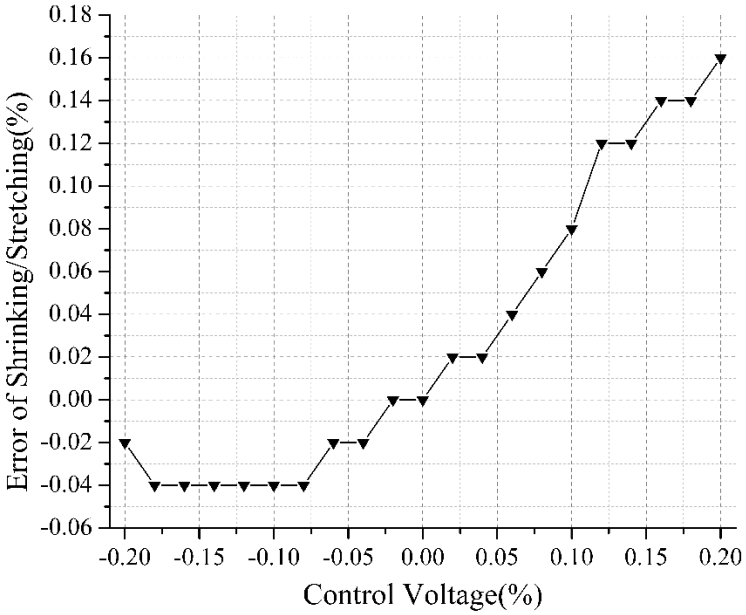
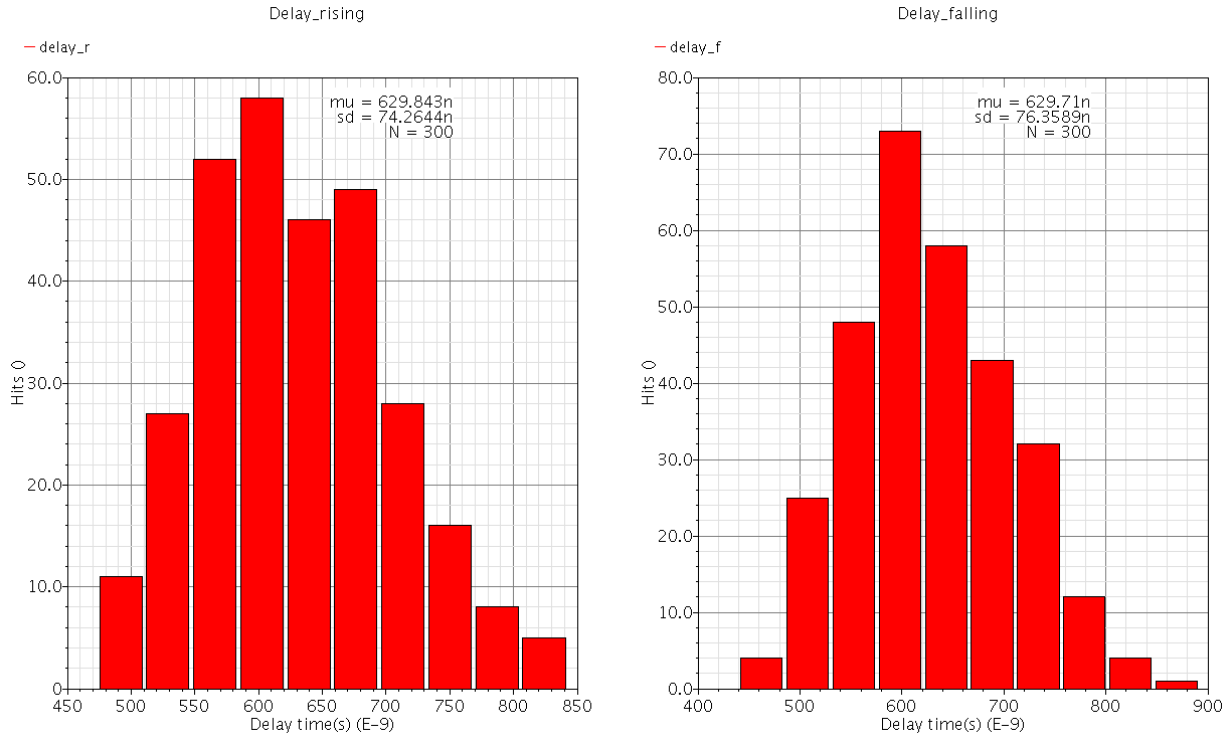


Figure 0-22: Pulse width shrinking/stretching variation of the VCDL

Another critical issue of the delay line in practical is the process variation and mismatch. Fig. 5-23 shows Monte Carlo simulation for the proposed VCDL. The typical value of the delay time is 630ns (the limit cycle frequency is over 200kHz), and the worst case is that the delay time is changed to 850ns. In that case, the limit cycle frequency will reduce to 150kHz. Therefore, in practical design, we need to leave more design space for the limit cycle frequency.



(a) (b)

Figure 0-23: Monte Carlo simulation of the delay line: (a) delay time for rising edge; (b) delay time for falling edge

Fig. 5-24 shows Monte Carlo simulation for delay time mismatch of the VCDL. The input signal is a square wave with duty cycle of 50%. Note that in the worst case is the pulse width will shrink or stretch 3%. And the error of over 79% of the hits is within 1%.

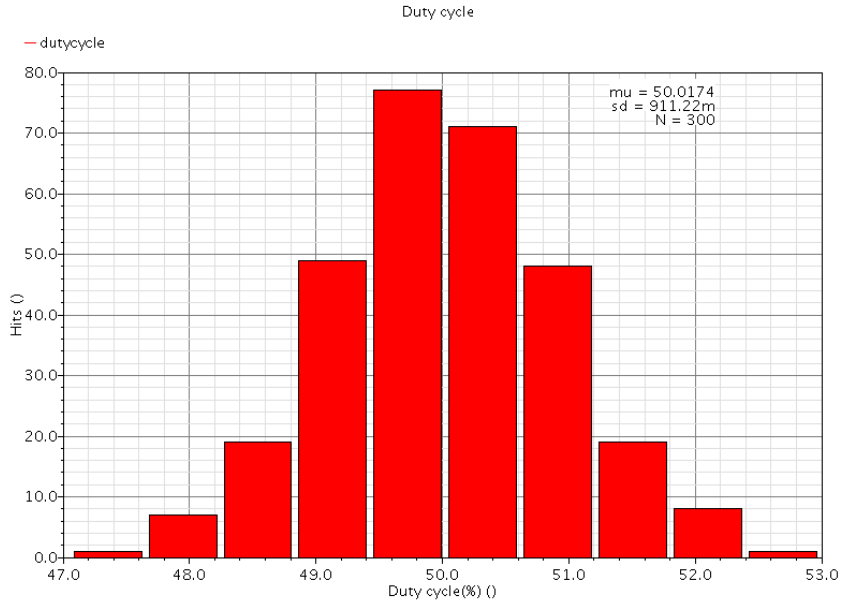


Figure 0-24: Monte Carlo simulation for shrinking/stretching of the delay line

Table 5-6 summarizes the target values imposed to the parameters of the voltage controlled delay line.

Table 0-6: Electrical simulation results for VCDL

Parameters	Value
Delay time(zero input)	$0.63\mu s$
Input dynamic range	$-200mV \sim 200mV$
Pulse shrinking/stretching	$< 0.5\%$

1.21.3 Transistor-level simulation

The comparison between the proposed ASDM and conventional one is shown in Fig. 5-25. The limit cycle frequency both proposed and conventional ASDM is set to be higher than 200kHz (maximum 224kHz). When the maximum signal amplitude is applied, the output instantaneous frequency of the conventional ASDM drops to 80kHz. While for the proposed one, the output instantaneous frequency maintains to be over 200kHz over the entire input range.

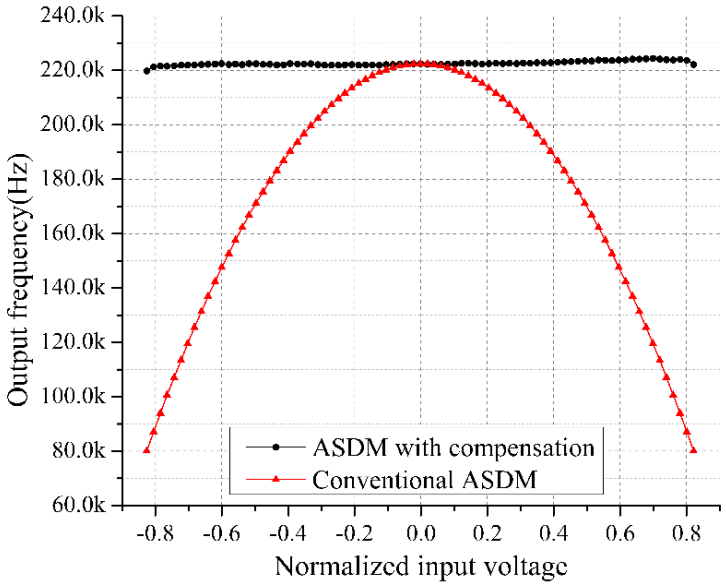


Figure 0-25: Comparison of the output instantaneous frequency between the conventional ASDM and the proposed one

The stability of the output frequency is shown in Fig. 5-26. For the full range normalized input, the variation of the frequency is within 1.2%. While for the normalized input range from -0.4 to 0.4, the variation is within 0.25%. In that case, the proposed ASDM can be considered as an ideal pulse width modulator (PWM). The linearity of the proposed ASDM is shown in Fig. 5-27. Clearly the normalized error of the duty cycle is within 0.1% for the full range input.

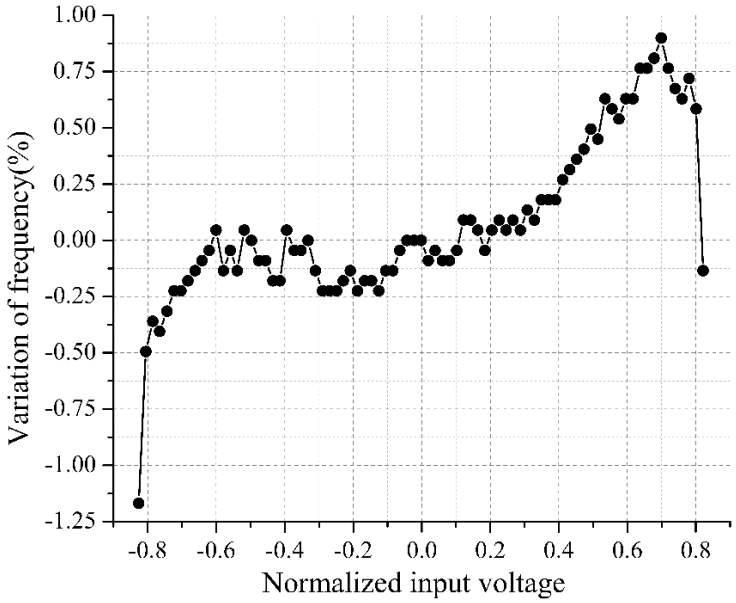


Figure 0-26: Stability of the frequency in the proposed ASDM

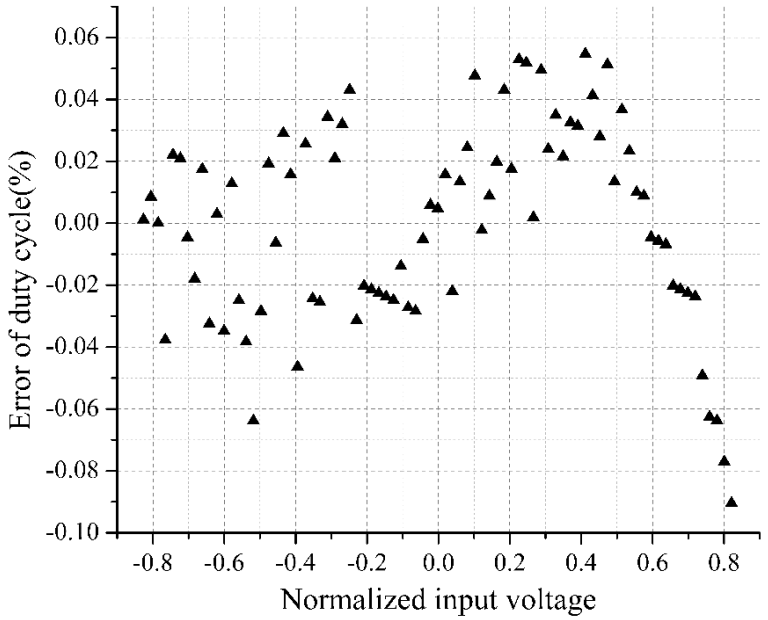


Figure 0-27: Normalized error of the duty cycle of the proposed ASDM

The PSD of the proposed ASDM is shown in Fig. 5-28. Compared with Fig. 5-1, with the benefit of the frequency compensation, the number of limit cycle spectral components is reduced, and they are much further away from signal baseband. Therefore, the requirement of the limit cycle frequency of the proposed ASDM is reduced. In other words, the signal bandwidth of the proposed ASDM can be at least doubled with the same limit cycle frequency. The SFDR of the proposed modulator is over 72.4dB with signal bandwidth of 6kHz.

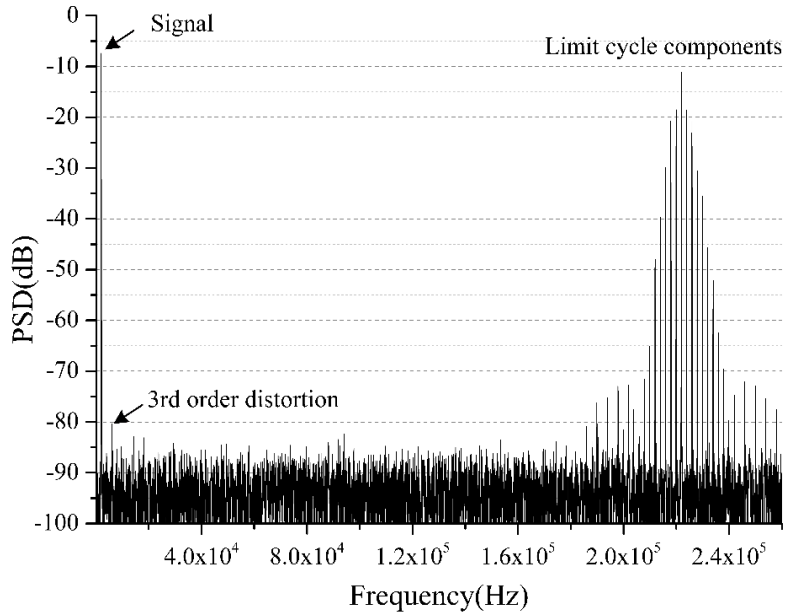


Figure 0-28: PSD of the proposed ASDM ($f_c/2B=16$)

1.22 Summary

In this chapter, a novel asynchronous sigma delta modulator with frequency compensation is presented. The proposed ASDM implements a source controlled delay cell instead of the hysteresis in the comparator to control the limit cycle frequency. The purpose of this proposed modulator is to apply compensation so as to stabilize the instantaneous output frequency. The compensation block is realized by an improved voltage controlled delay cell, which comprises a voltage-to-current converter, a translinear loop and a current starving delay cell. The selecting path chooses the suitable control voltage in different phases, and feeds it to the voltage-to-current converter to generate a compensation current. A current mode translinear loop is used to generate a control current for the delay cell in order to achieve linear delay control.

The proposed asynchronous sigma delta modulator achieves a higher accuracy than the conventional one in the signal band, as demonstrated by theoretical analysis. This is also demonstrated by simulation. According to Cadence Spectre transistor-level simulation, the variation of the output frequency is within 1.2% for full range input ($V = 0.8$), and the non-linear error is within 0.1%. The proposed ASDM can realize a significantly wider signal bandwidth with the same limit cycle frequency than the conventional ASDM. According to the simulation results, the signal bandwidth of the proposed ASDM is 6kHz with SFDR over 72.4dB.

Conclusions

1.23 Conclusion

This work studied a new type of sigma delta modulators, known as the asynchronous sigma delta modulator, where the sampled quantiser is replaced by a continuous-time comparator with hysteresis. As the main advantages of using an asynchronous sigma delta modulator instead of the synchronous continuous-time sigma delta modulator we highlight the following:

- Much simpler configuration. For the conventional synchronous continuous-time sigma delta modulators, at least a second or high order loop filter is required to obtain a high resolution. Additionally, in order to improve stability, a multi-bit quantiser is normally implemented, which requires an equivalent multi-bit DAC in the feedback loop. In asynchronous sigma delta modulators, a first order loop filter is enough to achieve a high resolution. As signal information is converted into time signal, the two-level comparator does not cause the instability problem.

- Absence of a sampling clock. Because of the absence of the clock speed constraint, asynchronous sigma delta modulators can, in theory, achieve an ultra-wide bandwidth.

- Clock jitter immunity. As there is no sampling process and DAC in the loop, asynchronous sigma delta modulators are immune to the clock jitter.

- Low power consumption.

On the other hand, asynchronous sigma delta modulators also have several issues, which influence the circuit design and applications. These are:

- Limit cycle components, which reduce the effective signal bandwidth and require a high order filter.

- Lack of noise shaping, so that a high resolution decoding circuit is required to maintain the performance of the modulator.

- Distortion due to:
    - Finite limit cycle frequency
    - Propagation loop delay

The main contributions of the thesis are:

1. Systematic analyse the non-ideal performance of asynchronous sigma delta modulators, including the non-deal integrator, propagation loop delay.

2. Introduction of a new effective decoding solution for asynchronous sigma delta modulators. The decoding circuit implements a special coarse-fine time-to-digital converter to quantise the square wave produced by asynchronous sigma delta modulators, and converts the duty cycle to a digital output. The time-to-digital converter operates asynchronously by utilizing vernier delay lines. The purpose of this circuit is to achieve a high resolution with a low frequency sampling clock, which is suitable for the ultra-low power applications. The proposed circuit is designed in AMS $0.35\mu m$ CMOS process. Spectre simulations, show that an 11-bit resolution can be realized.

3. Proposed a novel architecture of asynchronous sigma delta modulators with noise shaping. The proposed modulator introduces an 8-phase sampler after the comparator as the quantiser. A single-bit digital-to-time converter rather than the conventional multi-bit DAC is implemented to reconstruct a feedback signal. According to Spectre/Cadence simulations the proposed modulator with noise shaping can achieved peak SNDR of 78.2dB, which is 22dB better than the conventional asynchronous sigma delta modulator which uses same sampler.

4. Developed a compensation methodology to realize an improved asynchronous sigma delta modulator with constant limit cycle frequency. The purpose of the frequency compensation is to make the instantaneous output frequency constant so as to minimize the effect of the limit cycle frequency components when a large signal is applied. The compensation circuit is realized by a special voltage controlled delay line, which the delay time is related to the input signal. The proposed ASDM is designed to have a 6kHz signal bandwidth with the carrier-to-bandwidth ratio ($f_c/2B$) of 16. Spectre/Cadence simulation demonstrate a non-linear error is less than 0.1% with full range input from -200mV to 200mV. The variation of the output frequency is within 1.2% for full range input. The SFDR of the proposed ASDM is over 72.4dB.

The first chip of asynchronous sigma delta modulators was fabricated by Philips 8 years ago. The test results did show some attractive properties, such as better resolution than flash ADCs and lower power dissipation than CT-SDMs [49]. However, the development of ASDMs is not remarkable. This is because it requires a high frequency sampling clock to digitise the output signal, especially for bluetooth and WIFI applications. Unfortunately, this is limited by the current CMOS process. Now, with solutions of the decoding scheme and noise shaping shown in this thesis, ASDMs have opportunities to implement in these applications in a modern CMOS process. Moreover, the ASDM can also be applied on biomedical applications, where the SAR ADC is the only option in this application right now. Currently, many researchers focus on using CT-SDMs in this application. However, there is still a long way to go for CT-SDMs because of their high power dissipation. Similar to the high frequency applications, I believe that ASDMs can also obtain a low power dissipation in ultra-low power applications. With the benefit of frequency compensation, the power dissipation in digital decimation can also be reduced. In the feature, ASDMs will become good choice to fill the gap between SAR ADCs and CT-SDMs, and the gap between flash ADCs and CT-SDMs as well.

1.24 Future work

For future investigation and future work the following aspects of the research are suggested:

1. The decoding methodology introduced in Chapter 3 can be implemented in high frequency applicants, and can be realized by FPGAs.

2. As very a few asynchronous sigma delta modulators are fabricated, the novel architectures introduced in Chapter 4 and Chapter 5 need to be verified on silicon.

3. The power dissipation advantage of ASDMs in biomedical applications is not verified on silicon. The architecture of ASDMs in Chapter 5 is suitable for low frequency applications. So in the feature, I will design a specific modulator for biomedical sensors, such as neural sensors and EGG.

4. Asynchronous sigma delta modulators can also be decoded through frequency measurement, which uses a highly accurate low frequency, such as a quartz clock, as a reference.

Appendix

Appendix I

1. DC analysis

The Fourier transfer of eq. (2-13) is:

$$C(\omega)=2\pi\left[V-(2\alpha-1)\right]\delta(\omega)F(\omega)-8\,\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\delta(\omega-n\omega_0)F(\omega) \qquad \text{(I-1)}$$

Where $\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\cos n\omega_0 t=\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}e^{jn\omega_0 t}$; $FT\left[V-(2\alpha-1)\right]=2\pi\left[V-(2\alpha-1)\right]\delta(\omega)$;

$F\left[\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}e^{jn\omega_0 t}\right]=2\pi\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\delta(\omega-n\omega_0)$; $FT\left[f(t)\right]=F(\omega)$;

Therefore the inverse Fourier transform is:

$$c(t)=\int_{-\infty}^{\infty}\left[V-(2\alpha-1)\right]\delta(\omega)F(\omega)e^{j\omega t}d\omega-\frac{4}{\pi}\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\int_{-\infty}^{\infty}\delta(\omega-n\omega_0)F(\omega)e^{j\omega t}d\omega \qquad \text{(I-2)}$$

$$\begin{aligned}&\int_{-\infty}^{\infty}\left[V-(2\alpha-1)\right]\delta(\omega)F(\omega)e^{j\omega t}d\omega=\left[V-(2\alpha-1)\right]F(0)\\&\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\int_{-\infty}^{\infty}\delta(\omega-n\omega_0)F(\omega)e^{j\omega t}d\omega=\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\left[F(n\omega_0)\times(\cos n\omega_0 t+j\sin n\omega_0 t)\right]\end{aligned} \qquad \text{(I-3)}$$

After by incorporation eq. (I-3) into eq. (I-2), eq. (2-16) is obtained.

2. Sine wave signal input

Again, the Fourier transfer of eq. (2-14) is:

$$C_m(\omega)=2\pi\left[V\cos\mu T_m-(2\alpha-1)\right]\delta(\omega-\mu)F(\omega)-8\,\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\delta(\omega-n\omega_0)F(\omega) \quad \text{(I-4)}$$

The inverse Fourier transfer is:

$$c_m(t)=\left[V\cos\mu T_m-(2\alpha-1)\right]F(\mu)e^{j\mu t}-8\,\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\delta(\omega-n\omega_0)F(\omega) \quad \text{(I-5)}$$

By keeping only the real part, eq. (I-5) can be rewritten as:

$$\begin{aligned}c_m(t)=&\left[V\cos\mu T_m-(2\alpha-1)\right]\times\left[\mathrm{Re}\,F(\mu)\cos\mu T_m-\mathrm{Im}\,F(\mu_s)\sin\mu T_m\right]\\&-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\times\left[\mathrm{Re}\,F(n\omega_0)\cos n\omega_0 t-\mathrm{Im}\,F(n\omega_0)\sin n\omega_0 t\right]\end{aligned} \quad \text{(I-6)}$$

After inserting the boundary conditions the following two equation are obtained:

$$\begin{aligned}-b=&\left[V\cos\mu T_m-(2\alpha-1)\right]\times\left[\mathrm{Re}\,F(\mu)\cos\mu t+\mathrm{Im}\,F(\mu)\sin\mu t\right]\\&-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\times\left[\mathrm{Re}\,F(n\omega_0)\cos\alpha n\pi+\mathrm{Im}\,F(n\omega_0)\sin\alpha n\pi\right]\end{aligned} \quad \text{(I-7)}$$

$$\begin{aligned}b=&\left[V\cos\mu T_m-(2\alpha-1)\right]\times\left[\mathrm{Re}\,F(\mu)\cos\mu t-\mathrm{Im}\,F(\mu)\sin\mu t\right]\\&-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\times\left[\mathrm{Re}\,F(n\omega_0)\cos\alpha n\pi-\mathrm{Im}\,F(n\omega_0)\sin\alpha n\pi\right]\end{aligned} \quad \text{(I-8)}$$

Where

$$\cos n\omega_0\left(-\frac{T_1}{2}+k(T_1+T_2)\right)=\cos n\omega_0\left(\frac{T_1}{2}+k(T_1+T_2)\right)=\cos\alpha n\pi\cos\alpha n\pi$$

and

$$\sin n\omega_0\left(\frac{T_1}{2}+k(T_1+T_2)\right)=-\sin n\omega_0\left(\frac{T_1}{2}+k(T_1+T_2)\right)=\sin\alpha n\pi$$

By addition and subtraction eq. (I-7) and eq. (I-8):

$$\begin{cases} \left[V\cos\mu T_m-(2\alpha-1)\right]\mathrm{Re}\,F(\mu)\cos\mu t=\dfrac{4}{\pi}\displaystyle\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\mathrm{Re}\,F(n\omega_0)\cos\alpha n\pi \\ \left[V\cos\mu T_m-(2\alpha-1)\right]\mathrm{Im}\,F(\mu)\sin\mu t-\displaystyle\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\mathrm{Im}\,F(n\omega_0)\sin\alpha n\pi=-\dfrac{\pi b}{4} \end{cases} \tag{I-9}$$

$$\mu\left(\pm\frac{T_1}{2}+k\left(T_1+T_2\right)\right)=\mu\left(\pm\frac{\alpha\pi}{\omega_0}+k\frac{2\pi}{\omega_0}\right) \tag{I-10}$$

If $\mu<<\omega_0$, we obtain the following approximate result:

$$\mu\left(\pm\frac{\alpha\pi}{\omega_0}+k\frac{2\pi}{\omega_0}\right)=\frac{\mu}{\omega_0}\left(\pm\alpha\pi+2\pi k\right)\to 0 \tag{I-11}$$

From this, eq. (2-20) is easily obtained.

$$\int\left(1-\frac{V^2+V^2\cos 2\mu t}{2}\right)dt=\left(1-\frac{V^2}{2}\right)t-\frac{V^2}{4\mu}\sin 2\mu t \tag{I-12}$$

Eq. (2-21) can be rewritten as:

$$y_1(t)=\frac{4}{\pi}\mathrm{Re}\,e^{i\frac{\pi V}{2}\cos\mu t}\,\mathrm{Re}\exp\left\{i\left[\omega_c\left(1-\frac{V^2}{2}\right)t-\frac{\omega_c V^2}{4\mu}\sin 2\mu t\right]\right\} \tag{I-13}$$

Here we implement the Jacobi-Anger expansion, which states that:

$$\exp\left[iz\sin(\phi)\right]=\sum_{n=-\infty}^{\infty}J_n(z)e^{in\phi} \tag{I-14}$$

Eq. (2-22) follows.

3. Distortion

The Taylor series for a $\sin x$ is:

$$\sin x = x - \frac{(x)^3}{3!} + \frac{(x)^5}{5!} - \frac{(x)^7}{7!} \cdots \tag{I-15}$$

$$\sum_{n=1,3,5\cdots}^{\infty} (-1)^n \sin v_{in} \approx -\frac{1}{6}\left(v_{in} - {v_{in}}^3\right) \text{ [87]} \tag{I-16}$$

By inserting $v_{in} = V \cos \mu t$, eq. (2-23) can be easily obtained.

Appendix II

The Fourier transfer of $c(t)$ with the propagation loop delay $\Delta\tau$ can be written as:

$$\begin{aligned} C(\omega) = {} & 2\pi\left[V\cos\mu_s t-(2\alpha-1)\right]\delta(\omega-\mu_s)F(\omega) \\ & -8\,\mathrm{Re}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}\cos n\omega_0\Delta\tau\,\delta(\omega-n\omega_0)F(\omega) \end{aligned} \tag{II-1}$$

Hence, $c(t)$ can be obtained:

$$\begin{aligned} c(t) = {} & \left[V\cos\mu_s t-(2\alpha-1)\right]\times\mathrm{Re}\,F(\mu_s)-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n} \\ & \times\left[\mathrm{Re}\,F(n\omega_0)\left(\cos n\omega_0 t\cos n\omega_0\Delta\tau+\sin n\omega_0 t\sin n\omega_0\Delta\tau\right)\right. \\ & \left.+\,\mathrm{Im}\,F(n\omega_0)\left(\sin n\omega_0 t\cos n\omega_0\Delta\tau-\cos n\omega_0 t\sin n\omega_0\Delta\tau\right)\right. \end{aligned} \tag{II-2}$$

Because of the overshoot, the boundary conditions for the system with propagation delay can be expressed as:

$$\begin{cases} y(t_1)=1, c(t_1)=b_1, t_1=-\dfrac{T_1}{2}+k(T_1+T_2)+\Delta\tau \\ y(t_2)=-1, c(t_2)=-b_2, t_2=\dfrac{T_1}{2}+k(T_1+T_2)+\Delta\tau \end{cases} \tag{II-3}$$

Where $b_1=b+\Delta\tau k\left(1+\dfrac{V}{\mu}\sin\mu T_m\right)$; $b_2=b+\Delta\tau k\left(1-\dfrac{V}{\mu}\sin\mu T_m\right)$; $k=1/RC$ is the integrator factor of the loop filter

Inserting eq. (II-3) into eq. (II-2) will result:

$$\begin{aligned} b+\Delta\tau k\left(1+\frac{V}{\mu}\sin\mu T_m\right) = {} & \left[V\cos\mu T_m-(2\alpha-1)\right]\times\mathrm{Re}\,F(\mu)-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n} \\ & \times\left[\mathrm{Re}\,F(n\omega_0)\left(\cos\alpha n\pi\cos n\omega_0\Delta\tau-\sin\alpha n\pi\sin n\omega_0\Delta\tau\right)\right. \\ & \left.+\,\mathrm{Im}\,F(n\omega_0)\left(-\sin\alpha n\pi\cos n\omega_0\Delta\tau-\cos\alpha n\pi\sin n\omega_0\Delta\tau\right)\right. \end{aligned} \tag{II-4}$$

$$-b-\Delta\tau k\left(1-\frac{V}{\mu}\sin\mu T_m\right)=\left[V\cos\mu T_m-(2\alpha-1)\right]\times\mathrm{Re}\,F(\mu)-\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin\alpha n\pi}{n}$$
$$\times\left[\mathrm{Re}\,F(n\omega_0)\left(\cos\alpha n\pi\cos n\omega_0\Delta\tau+\sin\alpha n\pi\sin n\omega_0\Delta\tau\right)\right. \quad \text{(II-5)}$$
$$\left.+\,\mathrm{Im}\,F(n\omega_0)\left(\sin\alpha n\pi\cos n\omega_0\Delta\tau-\cos\alpha n\pi\sin n\omega_0\Delta\tau\right)\right.$$

The limit cycle frequency can be rewritten as:

$$f_c=A_0\frac{bk}{4} \quad \text{(II-6)}$$

Where A_0 is the open loop gain.

After addition and subtraction eq. (II-4) and eq. (II-5), eq. (2-37) can be obtained.

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